Radiation Hardness Assurance Testing of Microelectronic Devices and Integrated Circuits: Radiation Environments, Physical Mechanisms, and Foundations for Hardness Assurance

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Abstract

This document describes the radiation environments, physical mechanisms, and test philosophies that underpin the radiation hardness assurance test methodologies presented in Parts A and B. The natural space radiation environment is presented, including the contributions of both trapped and transient particles. The effects of shielding on radiation environments are briefly discussed. Laboratory radiation sources used to simulate radiation environments are covered, including how to choose appropriate sources to mimic environments of interest. The fundamental interactions of radiation with materials via direct and indirect ionization are summarized. Some general test considerations are covered, followed by in-depth discussions of physical mechanisms and issues for total dose and single-event effects testing. The purpose of this document is to describe why the test protocols we use are constructed the way they are. In other words, to answer the question: “Why do we test it that way?”

I. Natural Space Radiation Environment

Microelectronic devices and integrated circuits (ICs) can be exposed to a wide range of radiation environments. The types of particles, their energies, fluxes, and fluences (or total dose) can vary considerably among the different radiation environments that electronics devices can be exposed to. These differences can lead to large variations in radiation-induced degradation. Moreover, devices that may be susceptible to radiation-induced degradation in one radiation environment may be robust in other radiation environments. The first step toward developing hardness assurance tests for a given radiation environment is to determine the nature of particles that electronic devices can be exposed to. In this section, we present an overview of the naturally-occurring space radiation environment.

The concentrations and types of particles in the natural space environment vary significantly with altitude, angle of inclination, recent solar activity, and amount of spacecraft shielding. As such, it is nearly impossible to define a ”typical” space environment. Particles present in the earth’s natural space radiation environment include 1) particles trapped by the earth’s magnetic field (primarily electrons and protons), 2) galactic cosmic rays, and 3) solar cosmic rays. In this section, some of the general properties of the natural space environment are presented.

A. Particles Trapped by the Earth’s Magnetic Field

The earth’s magnetic field creates a geomagnetic cavity known as the magnetosphere [1]. The magnetic field lines trap low-energy charged particles. These trapped particles consist primarily of electrons and protons, although some heavy ions are also trapped. The trapped particles gyrate spirally around the magnetic field lines and are reflected back and forth between the poles where the fields are confined. The motion of the trapped particles is illustrated in Figure 1 [1]. As charged particles gyrate along the magnetic field lines, they also drift around the earth with electrons drifting in an easterly direction and protons drifting in a westerly direction. The motion of charged particles forms bands (or domains) of electrons and protons around the earth and form the earth’s two primary radiation belts.

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy’s National Nuclear Security Administration under Contract DE-AC04-94AL85000.

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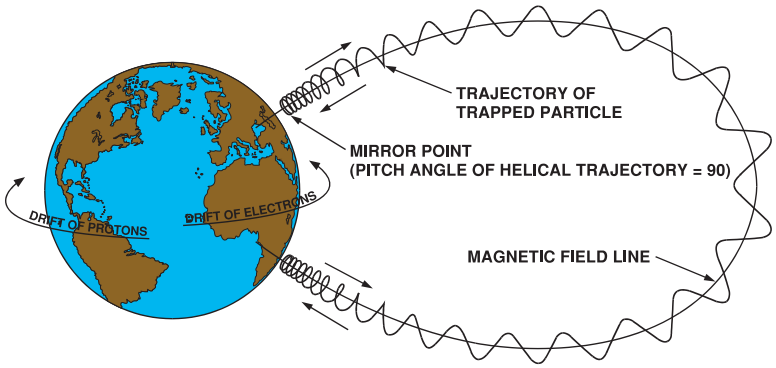

Fig. 1. Motion of trapped particles in the earth's magnetosphere. (After Ref. [1])

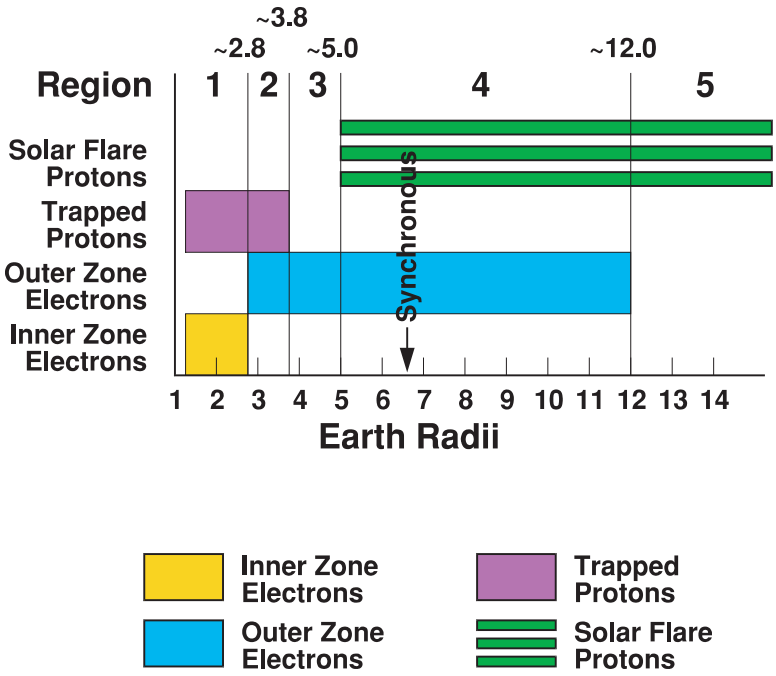

Fig. 2. Boundaries of the domains for solar flare and trapped protons and outer and inner zone electrons. (After Ref. [1])

The boundaries of the domains at the equator are illustrated in Figure 2 [1]. Distances are specified in earth radii (one earth radius is equal to 6380 km) referenced to the center of the earth, i.e., one earth radius is at the earth's surface. Because of variations in the magnetic field lines with latitude, the boundaries of the radiation belts vary with latitude (angle of inclination). Most satellites are operated in near-earth orbits at altitudes between about 1.2 and 10 earth radii. Geosynchronous orbit (GEO) is at an altitude of approximately 35,800 km, corresponding to approximately 6.6 earth radii. The domains can be divided into five regions. The trapped proton distribution exists primarily in regions one and two that extend from slightly above 1 earth radius to 3.8 earth radii (purple bar in Figure 2). The distribution of proton flux as a function of energy and radial distance is given in Figure 3 [1]. *[Flux is the rate at which particles impinge upon a unit surface area. It is normally given in units of particles/cm^2-s. The time integral of flux is fluence. Thus, fluence is equal to the total number of particles that impinge upon a unit surface area and it is normally given in units of particles/cm^2.]* Trapped protons in the earth's magnetosphere can have energies as high as 500 MeV [1]. Note that the altitude corresponding to the peak in flux decreases with proton energy. Protons with energies greater than 10 MeV primarily occupy regions one and two below 3.8 earth radii [1]. Typical spacecraft shielding attenuates protons with energies below 10 MeV [2]. Thus, the predominantly low-energy trapped protons present above 3.8 earth radii are normally ineffective in producing radiation-induced damage. For proton energies greater than 30 MeV, the highest proton flux occurs at about 1.5 earth radii. Protons originating from solar flares (discussed below) are present predominantly in regions four and five (Figure 2) and extend from $\sim$5 earth radii to beyond 14 earth radii.

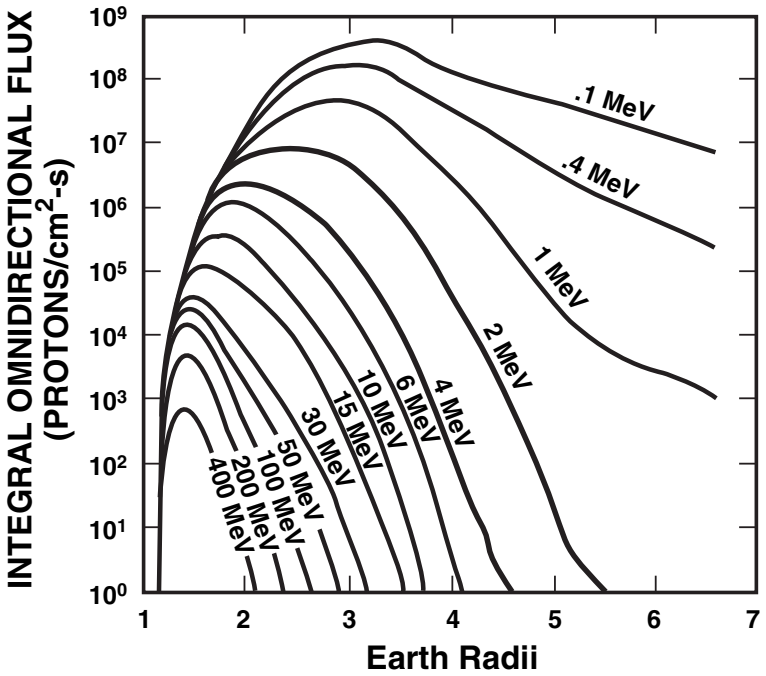

Fig. 3. Distribution of proton flux as a function of energy and radial distance. (After Ref. [1])

Above the Atlantic Ocean centered off the coast of South America, the geomagnetic sphere dips toward the earth, causing a region of increased proton flux at relatively low altitudes. This region is called the South Atlantic anomaly (SAA), and exists because of the difference between the earth's geographic spin axis and its magnetic axis [3]. In this region, the flux of protons with energies greater than 30 MeV can be as much as 10^4 times higher than in comparable altitudes over other regions of the earth. At higher altitudes, the magnetic sphere is more uniform and the South Atlantic anomaly disappears [3], [4]. Figure 4 shows maps of the proton belt structure at altitudes of 500 km, 1000 km, and 3000 km, clearly indicating the location of the SAA at low altitudes and the emergence of the background Van Allen belt structure at 3000 km [3].

Electrons are present predominantly in regions one to four and extend up to 12 earth radii [1]. The electron domain is divided into two zones, an inner zone extending to about 2.8 earth radii and an outer zone extending from 2.8 to 12 earth radii. The outer zone electrons have higher fluxes ($\sim$10 times) and energies than the inner zone electrons. For electrons with energies greater than 1 MeV, the peak in flux is located between 3 and 4 earth radii. The maximum energy of trapped electrons is approximately 7 MeV in the outer zone; whereas, the maximum energy is less than 5 MeV for electrons in the inner zone [1]. At these energies, electron interactions are unimportant for single-event effects, but must be considered in determining total-dose effects.

Fluxes of electrons and protons in particular orbits can be estimated from existing models. Two models that have been used to estimate proton and electron fluxes as a function of satellite orbit are AP8 [5] for protons and AE8 [6] for electrons. However, experimental data indicate that trapped particle populations are highly dynamic. Indeed, large solar events are known to have created temporary proton belts and have enhanced the electron belts [7]–[9]. These results indicate that the static AP8 and AE8 models may significantly underestimate the concentration of protons and electrons, especially for orbits between 1.8 and 3 earth radii. New, dynamic models of the trapped particle radiation environment are being developed to describe the solar-modulated environment more accurately [10], [11].

B. Galactic Cosmic Rays

Galactic cosmic rays originate from sources outside our solar system and are always present. In the absence of solar activity, cosmic radiation is composed entirely of galactic radiation. Outside of our solar system, the spectrum of galactic cosmic rays is believed to be uniform. Its composition as a function of atomic mass is given in Figure 5 [2], [12]. It consists mostly of protons (85%) and alpha particles (helium nuclei) (14%). Less than 1% of the galactic cosmic ray spectrum is composed of high-energy heavy ions. However, this is not an indication that heavy

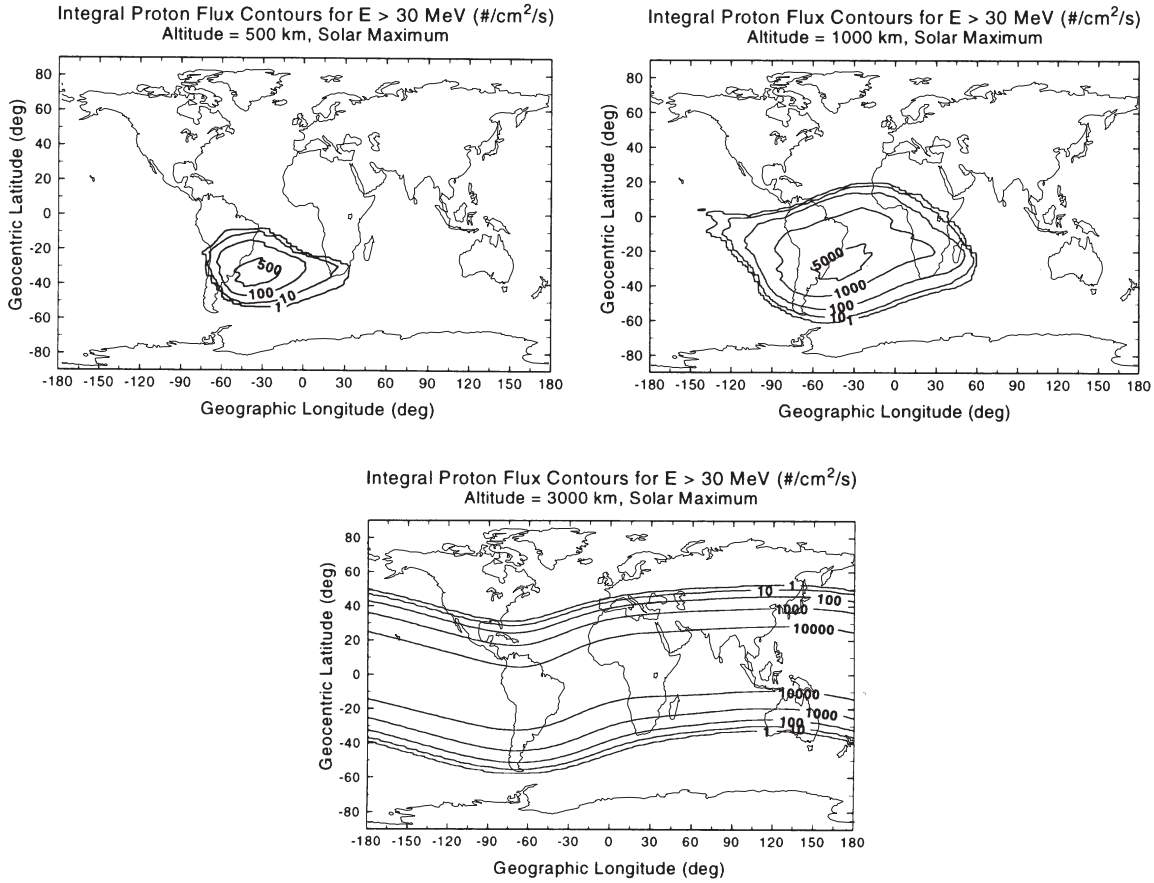

Fig. 4. Integral proton flux contours as a function of latitude and longitude at 500 km, 1000 km, and 3000 km. (After Ref. [3])

ions are not as important as protons in space radiation effects. As will be discussed below, heavy ions deposit more energy per unit depth in a material than protons, and can actually cause greater numbers of single-event effects than protons. As illustrated in Figure 5, the flux of protons is more than two orders of magnitude higher than the flux of either carbon or oxygen, and approximately five orders of magnitude higher than the flux of nickel. The energy spectrum of galactic cosmic rays is given in Figure 6 [13]. Note that the x axis of Figure 6 is given in units of MeV/nucleon. Thus, for carbon with 12 nucleons, the point at 100 MeV/nucleon on the x-axis corresponds to an energy of 1.2 GeV. For most ions, the flux peaks between 100 and 1000 MeV/nucleon. For carbon, the peak flux is at an energy of approximately 2.4 GeV. For protons and alpha particles, the energy of the ion can be more than 100 GeV/nucleon. At these high energies, it is nearly impossible to shield electronics inside a spacecraft from cosmic rays.

At geosynchronous orbit (35,800 km), the earth's magnetic field is weak enough that, for all practical purposes, it can be considered to have a negligible effect on the galactic cosmic ray spectrum [14]. However, as cosmic rays penetrate deeper into the magnetosphere, low-energy particles are attenuated, modifying the cosmic ray spectrum. Only the more energetic particles are able to penetrate the magnetosphere. The amount of geomagnetic shielding decreases with higher inclination orbits as the magnetic field lines converge near the poles.

C. Solar Particle Events

The frequency and severity of solar particle events is naturally dependent on the amount of solar activity. Solar particle events (most commonly referred to as solar flares, but also including larger events such as coronal mass ejections) are random in nature, but follow the $\sim$11-year cycle of solar activity. Figure 7 shows solar event proton fluences for solar cycles 20-22, superimposed over a plot of the sunspot number [3]. The cyclical variation of the sunspot number is readily apparent, as is the fact that most (but not all) high-fluence proton events occur during solar active years. Interestingly, the galactic cosmic ray flux is anti-correlated to the solar cycle, with maximum galactic cosmic ray flux occurring during solar minimum conditions. After a solar flare occurs, particles begin to

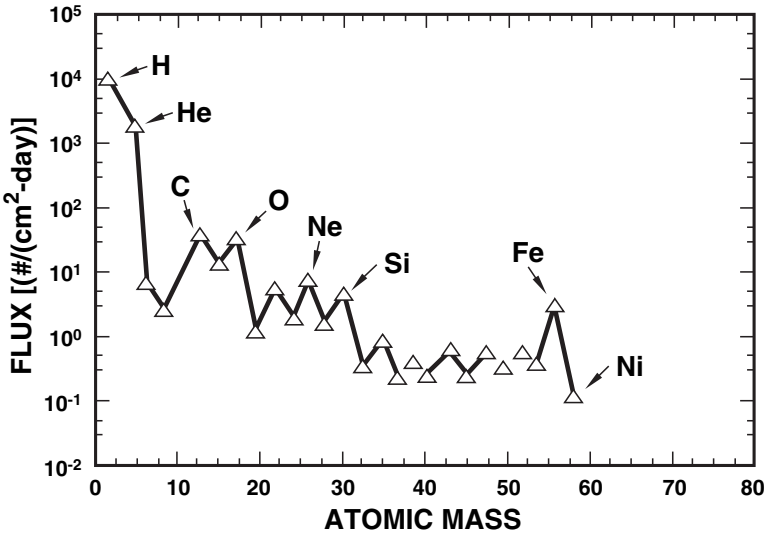

Fig. 5. Flux of galactic cosmic ray particles for atomic masses up to 59. (After Refs. [2] and [12])

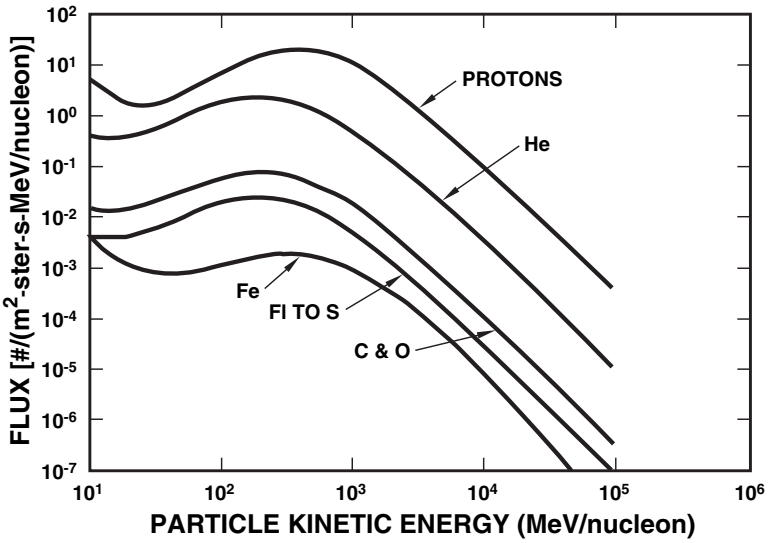

Fig. 6. Energy spectrum of galactic cosmic rays. (After Ref. [13])

arrive near the earth within tens of minutes, peak in intensity within two hours to one day, and are gone within a few days to one week (except for some solar flare particles which are trapped in the earth's radiation belts). In a solar flare, energetic protons, alpha particles and heavy ions are emitted. In most solar flares, the majority of emitted particles are protons (90-95%) and alpha particles. Heavy ions constitute only a small fraction of the emitted particles, and the number of heavy ions is normally insignificant compared to the background concentration of heavy ions from galactic cosmic rays. In a large solar flare, the number of protons and alpha particles can be greatly enhanced ($\sim 10^4$ times) over the background galactic cosmic ray spectrum; whereas, the number of heavy ions for a large solar flare approaches up to $\sim$50% of the background galactic cosmic concentration of heavy ions [13]. Associated with a solar flare is the solar wind or solar plasma. The solar wind usually arrives near the earth within one to two days after a solar flare [15]. As the solar wind strikes the magnetosphere, it can cause disturbances in the geomagnetic fields (geomagnetic storm), compressing them towards the earth. As a result, the solar wind can enhance the total dose received by devices in low-earth orbits.

Figure 8 is a plot of the angular flux of cosmic ray particles (both solar and galactic) during solar minimum and maximum inside a spacecraft in geosynchronous orbit with 25 mils of aluminum shielding as a function of linear energy transfer (LET) [16]. *[The term linear energy transfer (LET) is frequently used to describe the energy loss per unit path length of a particle as it passes through a material. LET has units of MeV-cm^2/mg. Because the*

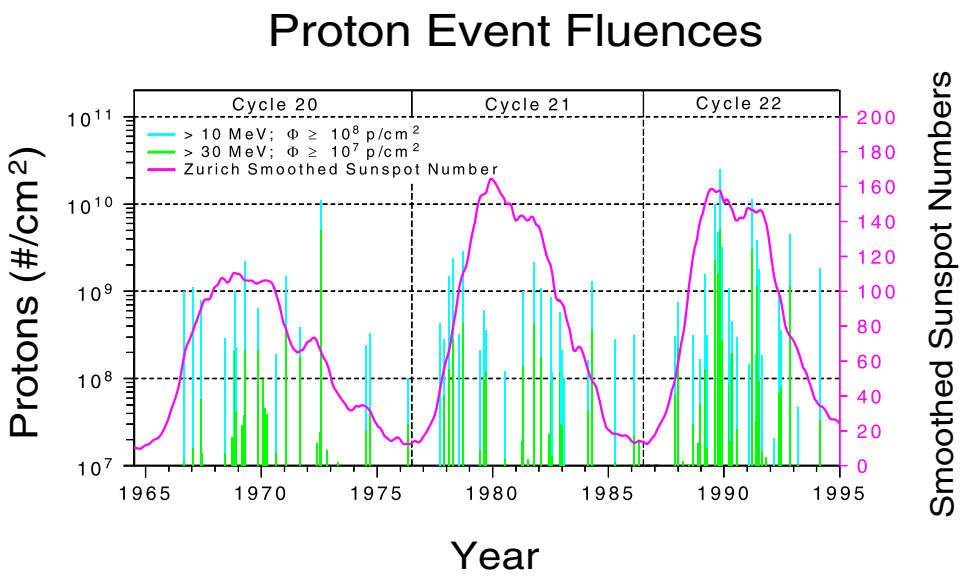

Fig. 7. Correlation of proton solar event fluence to sunspot number for solar cycles 20-22. Sunspot number is shown by the solid line plot, and proton solar event fluences by the vertical bars. (After Ref. [3])

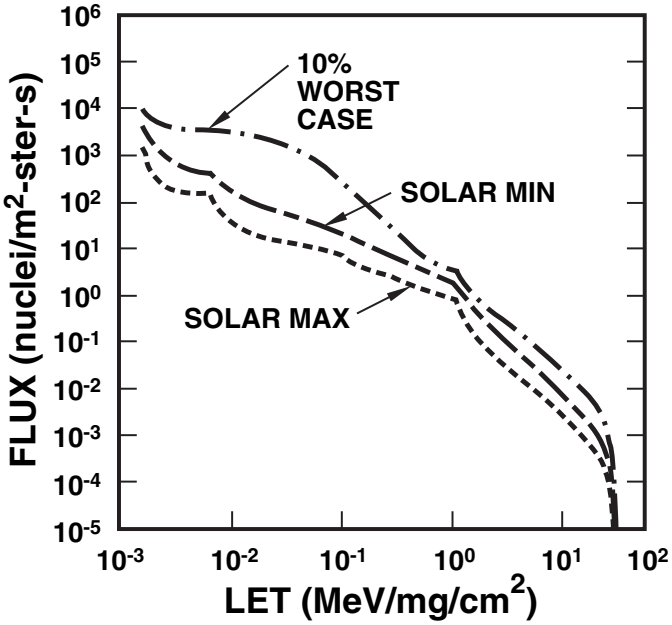

Fig. 8. Flux of cosmic ray particles at solar maximum, at solar minimum, and for Adams' 10% worst-case environment. (After Ref. [16])

energy loss per unit path length (in MeV/cm) is normalized by the density of the target material (in mg/cm^3), LET may be quoted roughly independent of the target. We can easily relate the LET of a particle to its charge deposition per unit path length. In silicon, an LET of 97 MeV-cm^2/mg corresponds to a charge deposition of 1 pC/μm. This conversion factor of about 100 is handy to keep in mind to convert between LET and charge deposition.] As shown in Figure 7, the solar cycle peaks in intensity approximately every 11 years. Solar maximum refers to periods of maximum solar activity, and solar minimum refers to periods of minimum solar activity. The solar wind during periods of high solar activity reduces the galactic cosmic ray flux. Thus, the minimum in galactic cosmic ray flux occurs during solar maximum, and the maximum in galactic cosmic ray flux occurs during solar minimum. The flux at solar minimum describes the actual environment for ~40% of the time. Also shown in Figure 8 is the Adams' 10% worst-case environment [16]. The actual environment is more intense than the Adams' 10% worst-case environment only 10% of the time. It includes contributions from both galactic and solar cosmic rays. This environment is often used in benchmarking the single-event upset hardness of electronic devices.

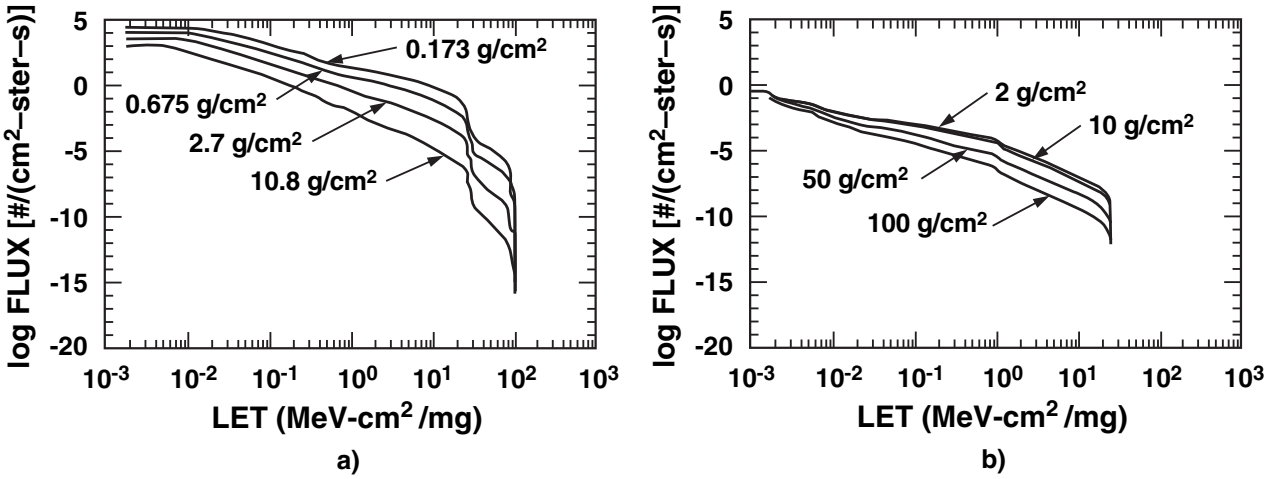

Fig. 9. The effects of aluminum shielding on the attenuation of the flux from a large solar flare (a) and of the flux from the galactic cosmic ray spectrum (b) as a function of the LET of the incident particles. (After Ref. [17])

D. Radiation Environment Inside a Spacecraft

Thus far, we have explored the natural space radiation environment outside a spacecraft. To determine the effects of the natural space environment on electronics inside the spacecraft, the effects of shielding must be taken into account. Shielding not only modifies the radiation environment inside a spacecraft by altering the energy and concentration of incoming particles, but also can create secondary particles as the incoming particles pass through the shielding. For instance, bremsstrahlung radiation in the form of x rays is emitted as energetic electrons decelerate in the shielding. For modest amounts of shielding, the effects of shielding can be estimated by taking into account only the energy loss of particles as they pass through the shielding [16].

The amount of energy loss as a particle passes through shielding depends on the thickness of the material. Typical spacecraft shielding is in the range of 100 to 250 mils. Figure 9a is a plot of flux for a large solar flare versus LET for aluminum thicknesses of 0.173 (25 mils) to 10.8 g/cm^2 (1570 mils) [17]. Note that increasing aluminum thickness results in decreasing solar flare flux for the relatively low-energy particles associated with a solar flare. However, the qualitative variation in flux with LET is relatively unaffected by the shielding. For LETs above 30 MeV-cm^2/mg, increasing the shielding thickness from 0.17 g/cm^2 to 10.8 g/cm^2 reduces the intensity of the spectrum by five orders of magnitude. The effect of spacecraft thickness on galactic cosmic ray flux is shown in Figure 9b [17]. It takes much more shielding to reduce the intensity of galactic cosmic rays. Spacecraft thicknesses of aluminum from zero up to 10 g/cm^2 (1450 mils) only slightly affect the LET spectrum. By comparing Figures 9a and b, we conclude that spacecraft shielding can attenuate the low-energy nuclei from a solar flare, but has little effect on the attenuation of nuclei in the galactic cosmic ray spectrum. Thus, for practical shielding thicknesses, additional shielding may prove effective against soft components of a solar flare environment, but is relatively ineffective in reducing the galactic cosmic ray spectrum [2].

Figure 10 is a plot of the contribution of protons, electrons, and bremsstrahlung radiation to the total dose received after a period of 139 days as a function of aluminum thickness measured aboard the Explorer 55 spacecraft [18]. The data were taken during a period of minimum solar activity. *[Note that the total dose is specified in units of rad(Al). A rad is defined as radiation absorbed dose. It is a measure of the amount of energy deposited in the material and is equal to 100 ergs of energy deposited per gram of material. The energy deposited in a device must be specified for the material of interest. Thus, for a MOS transistor, total dose is measured in units of rad(Si) or rad(SiO_2).]* For small aluminum thicknesses, both electrons and protons contribute to the total absorbed dose, while the contribution of bremsstrahlung radiation is negligible for all aluminum thicknesses. However, for aluminum thicknesses greater than $\sim$150 mils, the electron contribution to the total dose is negligible. Because of this, additional localized "spot" shielding near sensitive devices is sometimes used to reduce the total dose contribution from electron environments. However, increasing the shielding thickness from 100 to 250 mils of aluminum decreases the proton dose by less than a factor of two. Spot shielding is therefore less effective at mitigating total absorbed dose in proton-rich environments. Although these data are for a specific satellite orbit, the trends indicated in Figure 10 are typical for

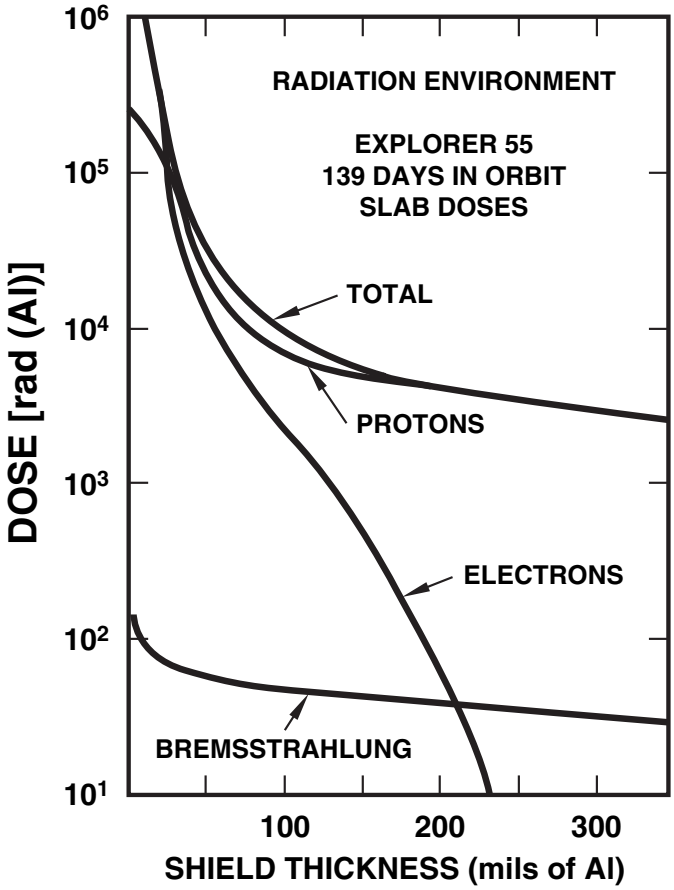

Fig. 10. Contributions of protons, electrons, and bremsstrahlung to total dose as a function of aluminum shielding. The data were taken after a 139-day exposure during the Explorer 55 space mission. (After Ref. [18])

those of other orbits.

As is apparent from Figures 2 and 3, the total dose from trapped electrons and protons that a device is exposed to in a space environment is highly dependent on the orbit. To determine the total dose, one must include contributions from both electrons and protons. The dose rate can vary over a wide range, from less than 10^{-6} to mid 10^{-3} rad(Si)/s. For a five year mission life, these dose rates correspond to a total-dose range of less than 1 krad(Si) to more than 5 Mrad(Si). For low-earth orbits at high inclination, 200 mils of aluminum shielding can limit the total proton dose to less than 1 krad(Si) per year [19]. Other orbits can result in total doses several orders of magnitude higher. At altitudes corresponding to roughly 1/2 the altitude at geosynchronous orbit (near worst case), the total dose that a device can receive inside a spacecraft with light shielding can approach 1 Mrad(Si) per year [1].

II. Laboratory Radiation Sources

A wide range of laboratory sources are available to characterize the response of electronic devices in space and nuclear radiation environments. These sources include irradiation cells based on radioactive isotopes, sources based on the generation of x-rays, and particle accelerators.

A. Total Ionizing Dose Sources

For total-dose effects, radiation sources range from very high dose rate sources for characterizing device response in weapon environments to very low dose rate sources for investigating the basic mechanisms of radiation effects or for simulating the total-dose response of electronic devices in the natural space environment. The most common laboratory sources are moderate dose rate Co-60 and x-ray sources. Co-60 sources emit gamma rays with a nominal energy of 1.25 MeV at dose rates up to 400 rad(Si)/s. The U. S. military standard test guideline MIL-STD-883, Method 1019 specifies that standard laboratory acceptance testing be performed at dose rates from

Fig. 11. Total-dose laboratory sources. a) Gammacell 220 Co-60 Source Irradiation Cell. b) Aracor 4100 wafer-level X-ray Irradiator.

50 to 300 rad(Si)/s. Thus, Co-60 sources can normally meet these requirements. Another common type of laboratory source is the 10-keV x-ray source. Laboratory x-ray sources that can test unlidded packaged devices or devices on a wafer are available that can achieve dose rates from about 100 rad(SiO_2)/s to above 2000 rad(SiO_2)/s. The high dose rate of x-ray sources and the capability for testing at the wafer level allows for rapid feedback on radiation hardness during device fabrication [21]. Thus, wafer-level x-ray testing is often used for monitoring the parametric response of microelectronic test structures during device fabrication, while Co-60 testing is used for final radiation hardness assurance qualification testing of completed devices and ICs. Figure 11 shows examples of two moderate dose rate laboratory radiation sources: a Co-60 radioactive source irradiation cell, and a wafer-level x-ray irradiation cabinet.

Two high dose rate sources that can be used to investigate the total-dose and dose-rate response of electronic devices at short times after a pulse of radiation are electron linear accelerators (LINACs) and proton cyclotrons. Electron LINACs are pulse type sources with pulse widths ranging from less than 20 ns to more than 10 μs with energies from 10 MeV to more than 40 MeV. Dose rates greater than 10^{11} rad(Si)/s can be obtained from electron LINACs. Proton cyclotrons are quasi-continuous sources and can have dose rates as high as 1 Mrad(Si)/s with energies from around 40 MeV to greater than 200 MeV. For simulating low dose rate total-dose effects, Co-60 and Cs-137 sources are available. Cs-137 sources emit gamma rays with a nominal energy of 0.66 MeV. Dose rates below 0.01 rad(Si)/s can be obtained from Cs-137 radiation sources.

B. Single-Event Effects Particle Accelerators

There are a wide range of particle accelerators available for characterizing heavy ion and proton induced single-event effects. These sources vary widely in ion species, energy, and flux. A sampling of some of the most often-used accelerator facilities are shown in Table I. Three often used heavy ion sources in the U. S. are Brookhaven National Laboratory's Twin Tandem van de Graaff accelerator, Lawrence Berkeley Laboratory's 88-inch cyclotron, and Texas A&M's cyclotron at its Radiation Effects Facility. At the Brookhaven facility, available ions range from protons with energies of 30 MeV (maximum) and LETs of 0.02 MeV-cm^2/mg to gold with energies of 350 MeV and LETs of 81 MeV-cm^2/mg (in silicon at normal incidence and maximum energy). At Berkeley's facility, ions are available ranging from protons with energies of 60 MeV (maximum) and LETs of 0.009 MeV-cm^2/mg to bismuth with energies of 803 MeV and LETs of 95 MeV-cm^2/mg (in silicon at normal incidence and maximum energy). In addition to these facilities, other facilities are available in the U. S. and throughout the world for characterizing

the single-event upset properties of electronic devices. Similar ions and LETs can be obtained at Texas A&M. Of these three facilities, the highest ion energies can be obtained at Texas A&M. Ions with energies as high as 40 MeV/nucleon can be obtained at Texas A&M. Even at these high energies, the ion energies in space can be several orders of magnitude higher. For this reason, the very high energy heavy ions available at facilities such as Michigan State and Brookhaven's NASA Space Radiation Laboratory are of increasing interest.

A number of proton cyclotrons are available in the U. S. for characterizing proton-induced single-event effects. Two commonly used proton cyclotrons are the Indiana University Cyclotron Facility, and the Crocker Nuclear Laboratory at the University of California at Davis. At the Indiana University cyclotron, protons with maximum energy of 200 MeV can be obtained, with lower energy protons available by using either copper degraders, or beryllium degraders followed by momentum analysis to reduce beam energy spread. The usual beam spot size is up to 7 cm in diameter with uniformity better than 70%. The beam spot size can be restricted by the use of collimators; alternatively a beam spreader can be used to increase the beam spot size to about 30 cm. The UC-Davis cyclotron provides a maximum proton energy of 63 MeV, with energies as low as 1.25 MeV obtained by re-tuning the cyclotron. This cyclotron is useful for low-energy proton irradiations, but does not cover the entire range of interest for protons in the space environment. The TRIUMF Proton Irradiation Facility in Vancouver, Canada is nearly ideal for proton radiation effects studies, covering proton energies from less than 20 MeV up to 500 MeV, the complete energy range of interest for the natural space radiation environment.

TABLE I

SINGLE-EVENT EFFECTS TEST FACILITIES

Facility	Description	Energy Range	Reference	Contact
Brookhaven National Laboratory SEU Test Facility Upton, NY	Heavy ion Tandem van de Graaff	1-10 MeV/u	[20]	Chuck Carlson (631) 344-5261
Texas A&M University Cyclotron Institute College Station, TX	Heavy ion cyclotron	1-40 MeV/u	[21]	Henry Clark (979) 845-1411
Lawrence Berkeley National Laboratory 88-inch Cyclotron Berkeley, CA	Heavy ion cyclotron	4.5-16 MeV/u	[22], [23]	Peggy McMahan (510) 486-5980
Michigan State University National Superconducting Cyclotron Laboratory East Lansing, MI	Heavy ion cyclotron	80-170 MeV/u	[24]	Raman Anantaraman (517) 333-6337
Brookhaven National Laboratory NASA Space Radiation Laboratory Upton, NY	Heavy ion boosted synchrotron	200-1000 MeV/u	[25]	Betsy Sutherland (631) 344-3380
Indiana University Cyclotron Facility Bloomington, IN	Proton cyclotron	35-200 MeV	[26], [27]	Barbara von Przewoski (812) 855-2913
TRIUMF Proton Irradiation Facility Vancouver, BC, Canada	Proton cyclotron	20-500 MeV	[28], [29]	Ewart Blackmore (604) 222-7461
University of California at Davis Crocker Nuclear Laboratory Davis, CA	Proton cyclotron	1-63 MeV	[30], [31]	Carlos Castaneda (530) 752-4228
Francis H. Burr Proton Therapy Center Boston, MA	Proton cyclotron	15-230 MeV	[32], [33]	Ethan Cascio (617) 724-9529

C. Choosing a Radiation Test Source

A number of factors should be considered when choosing the radiation test source. These include the application radiation environment, the device type, and the type of test to be performed (e.g., total dose, single-event upset, single-event latchup, etc.) For example, for total dose testing of standard MOS ICs, Co-60 gamma testing at dose rates from 50 to 300 rad(Si)/s is often adequate for hardness assurance testing. However, for bipolar devices, which can exhibit enhanced low dose rate sensitivity (ELDRS), testing at lower dose rates more representative of the

space environment (e.g., 0.01 rad(Si)/s) may also be required. Similarly, because of proton nuclear interactions with the high-Z materials used to fabricate advanced ICs, proton-induced single-event latchup testing should be performed at the highest proton energy of the use environment. Testing at a facility with a relatively low proton energy (e.g., at the U. C. Davis Cyclotron which has a maximum proton energy of 63 MeV) may drastically underestimate the latchup probability in low-earth orbits. ICs fabricated using advanced technologies can contain numerous metal/insulator overlayers. Because of these overlayers, the energy of heavy ions used for single-event effects testing must be sufficient to penetrate deep into the semiconductor material with sufficient linear energy transfer (LET) to ensure that all mechanisms that can lead to single-event effects are captured. As a result, testing at heavy-ion facilities with low ion energies (e.g., the Brookhaven National Laboratory Tandem van de Graaff) may lead to erroneous results for some devices. These issues for choosing a radiation test source are discussed in more detail below. As a general rule, however, the best source is the source that most closely matches the anticipated use environment. Some radiation sources can more accurately reproduce device degradation in certain radiation environments, as discussed in Section V.D.

III. Interaction of Radiation With Materials

The manner in which different types of radiation particles interact with materials and their effects on electronic devices can vary considerably. Irradiating devices with different radiation particles but to the same fluence level (or total dose) can result in considerably different levels of radiation-induced degradation. Even irradiating devices with the same radiation particle but with different energies can result in considerably different levels of radiation-induced degradation. In this section, we cover the basics of the interaction of radiation with materials for the most common types of radiation particles in the natural space radiation environment, the nuclear radiation environment, and those used for hardness assurance testing. Knowledge of the interactions of radiation with materials is fundamental to the development of reliable hardness assurance test procedures.

A. Gamma and X-Ray Ionizing Radiation

Both x rays and gamma rays are used routinely for hardness assurance testing and process development. As x rays or gamma rays impinge on a material, they generate electron/hole pairs in the material by ionization. Because of the extremely high energies of the gamma rays and x rays of interest, each x ray or gamma ray can generate hundreds to thousands of electrons and holes. Whether the net effect of gamma-ray or x-ray exposure is the generation of photocurrents causing dose rate effects or the buildup of radiation-induced charge in oxides causing total dose effects, almost all of the net radiation-induced degradation is caused by the generated electrons and holes, i.e., very little of the radiation-induced degradation is directly caused by the incident gamma rays or x rays.

Photons interact with material through three different processes, namely the photoelectric (or fluorescent) effect, the Compton effect, and pair production [34]. These processes are illustrated in Figure 12. For each of these processes, the primary result of the interaction is the creation of energetic secondary electrons. Low-energy photons interact with material predominantly through the photoelectric effect. The photoelectric effect is illustrated in Figure 12a. In this process, an incident photon excites an electron from an inner shell of a target atom to a high enough state to be emitted free of the target atom. The incident photon is completely absorbed. Thus, the photoelectric effect creates a free electron (photoelectric electron) and an ionized atom. In addition, as the photoelectric electron is emitted, an electron in an outer orbit of the atom will fall into the spot vacated by the photoelectron causing a low-energy photon to be emitted. In general, the low-energy photon does not have sufficient energy to create additional electron-hole pairs, but depending on the energy of the incident photon, the emitted electron can generate numerous additional hole-pairs.

For higher-energy photons, Compton scattering will dominate over the photoelectric effect. Compton scattering is illustrated in Figure 12b. In this process, as a photon collides with an atom, the photon transfers a fraction of its energy to an electron of the target atom, giving the electron sufficient energy to be emitted free of the target atom. For Compton scattering, a photon of lower energy is created which is free to interact with other target atoms. It can also create a free electron and an ionized atom. Pair production occurs only for very-high energy photons ($E>3$ MeV). It is illustrated in Figure 12c. In pair production, the incident photon collides with a target atom creating an electron-positron pair. A positron has the same properties as an electron (charge and mass), except that the charge is positive. The incident photon is completely annihilated in pair production.

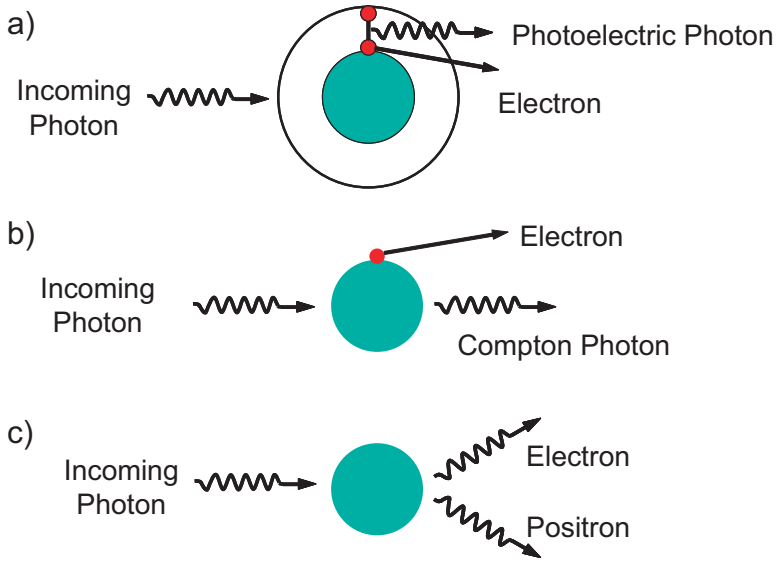

Fig. 12. Schematic drawing of three processes through which photons interact with material: a) photoelectric effect, b) Compton scattering, and c) pair production. (After Ref. [34])

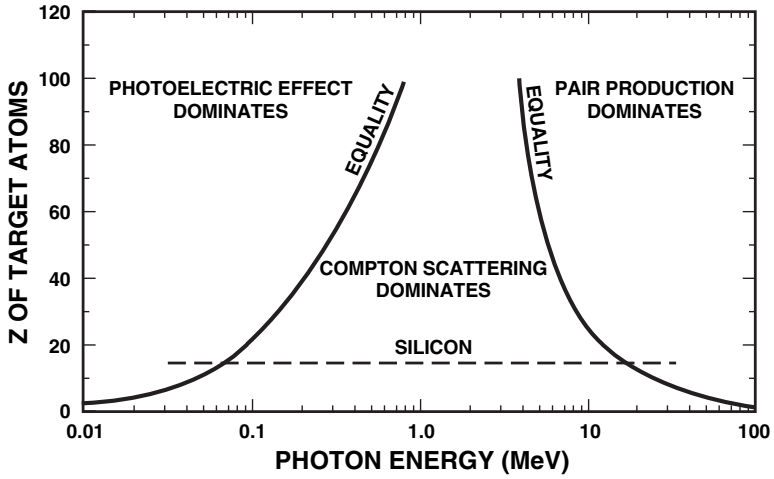

Fig. 13. Relative importance of the photoelectric effect, Compton scattering, and pair production as a function of photon energy. (After Ref. [35])

The relative importance of the three processes as a function of photon energy and atomic mass of the target material is illustrated in Figure 13 [35]. Shown in Figure 13 are regions where each process dominates. The solid lines correspond to equal probabilities for the different interactions. The dashed line corresponds to the atomic mass of silicon (Z=14). Thus for silicon, x rays emitted from a low-energy (typically 10 keV) x-ray irradiator will interact predominantly through the photoelectric effect, while high-energy gamma rays (typically 1.25 MeV) from a Co-60 source will interact predominantly through Compton scattering.

A mechanism that can result in differences in the number of electron/hole pairs generated by x rays or gamma rays is dose enhancement. Dose enhancement arises when an incident particle travels through two adjacent materials with different atomic masses. Close to the interface of two materials, charge particle equilibrium is not maintained. Charge particle equilibrium is defined as the condition where the total energy carried out of a given mass element by electrons is equal to the energy carried into it by electrons [36]. For two adjacent materials with different atomic masses, the number of electrons generated in the low-atomic mass material close to the interface will be higher than for the case where charge particle equilibrium is maintained (i.e., far away from the interface) as shown in Figure 14. This effect is called dose enhancement.

For thick oxides (Figure 14a), some dose enhancement in the SiO_2 occurs near the oxide interfaces (dashed lines), but for the majority of the oxide, the actual dose in the SiO_2 is close to its equilibrium dose (solid lines).

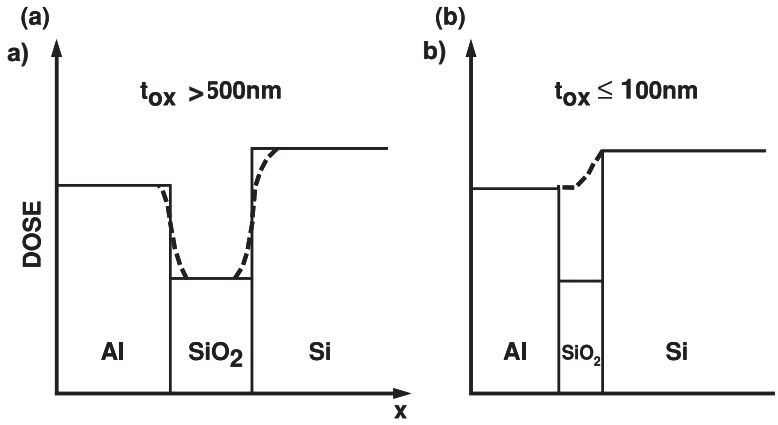

Fig. 14. Schematic diagram illustrating dose enhancement for a) a thick oxide ($t_{ox} > 500$ nm) and b) a thin oxide ($t_{ox} \leq 100$ nm). The solid lines indicate bulk equilibrium dose and the dashed lines indicate the actual dose profiles. (After Ref. [37])

For thin oxides (Figure 14b), the actual dose (dashed line) is considerably enhanced over the equilibrium dose. The criterion for thin or thick depends on the distance that secondary electrons will penetrate into the material. For 10-keV x rays in SiO_2, the average range of secondary electrons is approximately 500 nm. This distance is considerably longer than the gate oxide thickness of modern IC technologies and in many cases it is comparable to the thickness of field oxide isolation and the thickness of SOI buried oxides. Thus, significant dose enhancement effects can occur in most of the oxide structures of present-day IC technologies.

The amount of dose enhancement will depend on the mechanism by which an incident photon interacts with a material. It will be largest for low-energy photons ($\ll$1 MeV) which interact through the photoelectric effect [38]. For low-energy photons the number of secondary electrons generated is proportional to Z^4. Thus, as the atomic mass increases, the number of secondary electrons greatly increases. For an MOS transistor with a polysilicon gate, the atomic mass of silicon is slightly above the atomic mass of silicon dioxide and the amount of dose enhancement is negligible for 1.25-MeV Co-60 gamma rays (which interact through Compton scattering). On the other hand, for low-energy 10-keV x rays (which interact through the photoelectric effect) the amount of dose enhancement can be relatively large ($\sim$1.7) [37], [39], i.e., the dose in the oxide layer is 1.7 times the dose measured in charge particle equilibrium. Higher dose enhancement factors will result for metal silicide gates with higher atomic masses (e.g., tungsten and tantalum) [38], [40], if the distance of the metal layer from the oxide interface is within the range of the penetration depth of secondary electrons. For those materials in which significant dose enhancement can occur, the number of electron-hole pairs generated by the incident radiation must be multiplied by a dose-enhancement factor to determine the total number of electron-hole pairs generated.

B. Electron-Hole Pair Generation

High-energy electrons (secondary electrons generated by photon interactions or electrons present in the environment) and protons can ionize atoms, generating electron-hole pairs. As long as the energies of the electrons and holes generated are higher than the minimum energy required to create an electron-hole pair, they can in turn generate additional electron-hole pairs. In this manner, a single, high-energy incident photon, electron, or proton can create thousands of electron-hole pairs. The minimum energy required for creating an electron-hole pair, E_p, in silicon, silicon/dioxide and GaAs is given in Table II [34]. Also given in Table II are the densities for the three materials and the initial charge pair density per rad deposited in the material, g_0. The latter quantity is obtained from the product of the material density and the deposited energy per rad divided by E_p.

C. Energetic Particle Radiation

There are two primary methods by which energetic particle radiation releases charge in a semiconductor device: direct ionization by the incident particle itself, and ionization by secondary particles created by nuclear reactions between the incident particle and the struck device. Both mechanisms can lead to integrated circuit malfunction.

TABLE II

MINIMUM ENERGY FOR CREATING ELECTRON-HOLE PAIRS, DENSITY, AND PAIR DENSITY GENERATED PER RAD FOR GAAS, SILICON, AND SILICON DIOXIDE.

Material	E_p (eV)	Density (g/cm^3)	Pair density generated per rad, g_0 (pairs/cm^3)
GaAs	~4.8	5.32	$\sim 7\times10^{13}$
Silicon	3.6	2.328	4×10^{13}
Silicon Dioxide	17	2.2	8.1×10^{12}

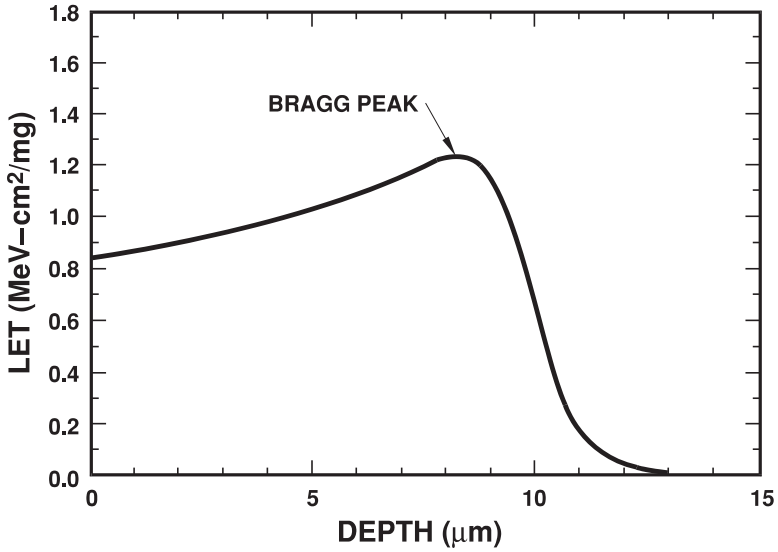

Fig. 15. Stopping power (LET) versus depth for a 2.5 MeV helium ion in silicon. (After Ref. [2])

1) Direct Ionization: When an energetic charged particle passes through a semiconductor material it frees electron-hole pairs along its path as it loses energy. If all of its energy is lost, the particle comes to rest in the semiconductor, having travelled a total path length referred to as the particle's range. Particle range is an important parameter that needs to be considered when performing heavy-ion testing in the laboratory. The range must be long enough to ensure that all mechanisms that can lead to single-event effects are captured. For the extremely energetic heavy ions in space, heavy ions are not routinely stopped in device materials. Direct ionization is the primary charge deposition mechanism for upsets caused by heavy ions, where we define a heavy ion as any ion with Z$\geq$2 (i.e., particles other than protons, electrons, neutrons, or pions). Lighter particles such as protons do not usually produce enough charge by direct ionization to cause upsets in memory circuits.

As a high-energy ion passes through a material, it loses energy by excitation and ionization of atoms, creating a very high density electron-hole plasma along the path of the ion. The amount of energy that an ion deposits per unit depth in a material is given by its stopping power. The mass-stopping power is defined as the linear energy transfer, LET, and is given by

$$LET = \frac{1}{\rho}\frac{dE}{dx} \tag{1}$$

where ρ is the density of the material and dE/dx is the rate of energy loss in the material. LET has the units MeV-cm^2/mg. The integral of LET over path length gives the total deposited energy. Figure 15 [2] is a plot of stopping power (LET) for 2.5-MeV helium ions as a function of depth in silicon. The point of maximum stopping power is called the Bragg peak. The LET for a given ion depends on the target material and energy. Stopping powers can be calculated for silicon, germanium, GaAs, and many compounds using the TRIM or SRIM code [41].

For single-event effects, an important parameter is the charge deposited in the material. The total deposited charge in a particle track, Q_l, can be calculated from

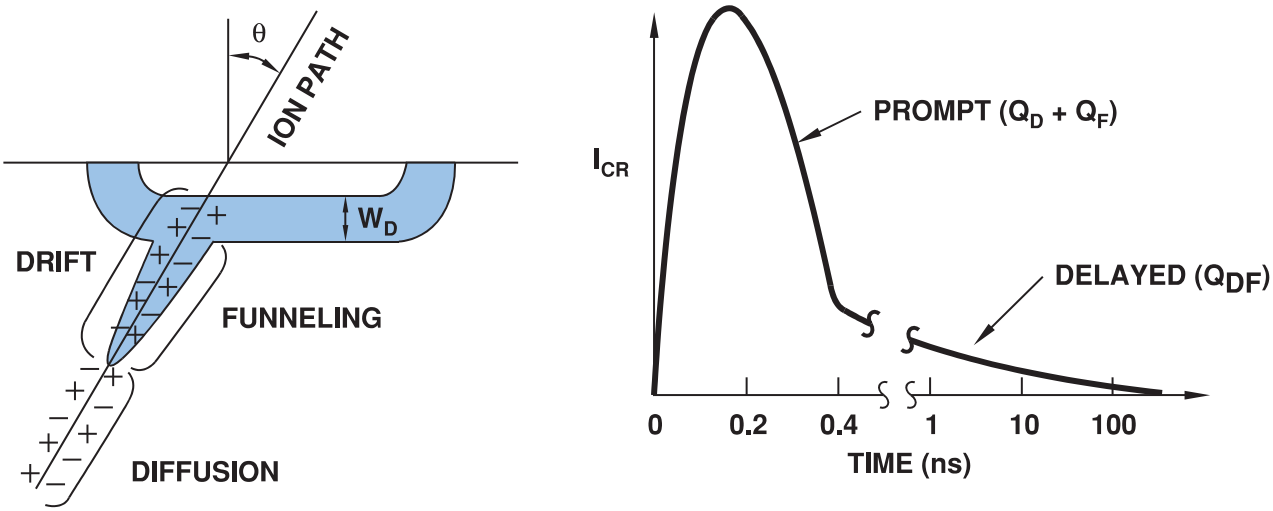

Fig. 16. Schematic diagram and time dependence for charge collection by drift, funneling, and diffusion. (After Ref. [2])

$$Q_l = \frac{1.6 \times 10^{-2} \cdot LET \cdot \rho}{E_p} \tag{2}$$

where E_p is the electron-hole pair ionization energy (minimum energy required to create an electron-hole pair) given in units of eV (see Table II), LET is in units of MeV-cm^2/mg, ρ is in units of g/cm^3, and Q_l is given in the units of pC/μm. For silicon, E_p = 3.6 eV and for GaAs, E_p = 4.8 eV. Thus, for an LET of 50 MeV-cm^2/mg, the charge deposited is approximately 0.5 pC/μm and 0.89 pC/μm in silicon and GaAs, respectively.

If the ion passes through a p-n junction, charge can be collected at the electrodes by drift of carriers from within the depletion region. The drift of carriers to the electrodes occurs within hundreds of picoseconds after a heavy-ion strike. This is depicted as Q_D in Figure 16. The amount of charge that is collected by drift of carriers within the depletion region can be greatly enhanced by "field funnelling." Funnelling was first observed by Hsieh, et al. in numerical simulations of the interaction of an alpha particle in a silicon junction diode [42]. The density of the electron-hole plasma (10^{18} to 10^{21} cm^{-3}) created by the ion strike is considerably greater than the doping concentration of typical p-n junctions [43]. The high concentrations of electron and holes in the plasma will distort the original depletion region of the junction along the path of the ion. As a consequence, the junction field region creates a "funnel region" that extends down into the substrate as depicted in Figure 16. The funnel will exist as long as the concentration of electron-hole pairs in the plasma created by the ion strike is large compared to the doping concentration of the substrate. As the original depletion region is re-established, the electric field sweeps through the funnel region, causing carriers to be collected rapidly by drift to the electrodes. For silicon devices, the amount of charge that is collected by drift can be enhanced by the funnel region, increasing the sensitivity of silicon ICs to single event upset. For SOI devices, because of the extremely thin silicon active layers used to fabricate transistors, funnelling effects are not important.

Diffusion of carriers to the edge of the junction depletion or funnel region contributes a another component to the collected charge. The diffusion of carriers takes much longer (nanoseconds to microseconds) than the drift component. The diffusion of carriers is noted as Q_{DF} in Figure 16.

The SEU sensitivity of an IC is normally characterized by measuring the upset cross section versus ion LET. The upset cross section usually has units of cm^2 or bits/cm^2. LET is varied by using different ions and by varying the angle of the incident ion beam normal to the device surface. By varying the angle of incidence, effectively more or less charge can be deposited per unit path length into the sensitive volume of the semiconductor device. The upset cross section curve can be roughly characterized by an LET threshold and a saturation upset cross section. To determine the number of circuit errors that will result for a space mission, one must convolve the upset cross section curve with the heavy-ion versus LET spectrum for the orbit. This is schematically illustrated in Figure 17. The error rate (in units of errors/bit-day) is calculated by taking into account the flux of particles in the environment and the upset cross section curve, which describes the device's sensitivity to that environment. With all else held constant, an increase in LET threshold and/or a decrease in the upset saturation cross section will lead to a decrease

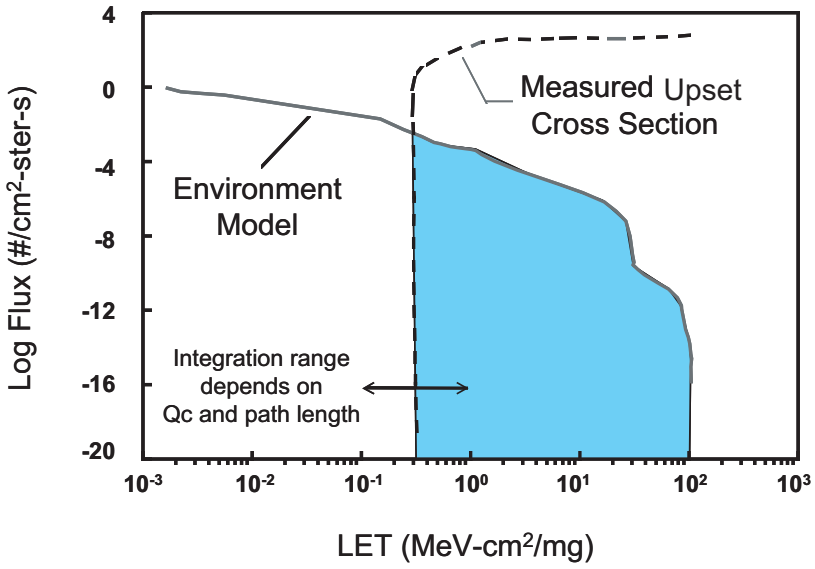

Fig. 17. Measured upset error cross section and particle flux for a hypothetical space environment. The error rate is determined by convolving the environment model with the error cross section. (After Ref. [2])

in the error rate. There are several software packages that one can use to calculate the heavy-ion or proton spectrum and predict the error rate in most earth-based satellite orbits [44], [45].

Other factors can also influence the amount of charge collected from a particle strike. For example, in silicon-on-insulator (SOI) technology, an attribute that limits the SEU hardness is the bipolar effect. This effect is due to a floating body (not referenced to a specific potential) in SOI transistors. A bipolar effect occurs in SOI transistors as a heavy-ion strike injects majority carriers in the body region of a transistor [46]–[48]. The injected charge must either recombine, be swept to the source junction, contribute to MOS channel charge, or exit through the distributed resistance of the body material. The latter current can lower the source-to-body potential causing minority-carrier injection from the source to the body where the injected carriers can be collected at the drain. This is analogous to minority carrier injection from the emitter-to-base region in a bipolar junction transistor. The bipolar current adds to (enhances) the charge collected by the normal drift of carriers generated by the ion strike. Once collected, the charge can lead to circuit upset.

2) Indirect Ionization: Although direct ionization by light particles does not usually produce enough charge to cause upsets, this does not mean that we can ignore these particles. Protons and neutrons can both produce significant upset rates due to indirect mechanisms. As a high-energy proton or neutron enters the semiconductor lattice it may undergo an inelastic collision with a target nucleus. Any one of several nuclear reactions may occur, including: (1) elastic collisions that produce Si recoils; (2) the emission of alpha or gamma particles and the recoil of a daughter nucleus (e.g., Si emits an alpha particle and a recoiling Mg nucleus); and (3) spallation reactions, in which the target nucleus is broken into two fragments (e.g., Si breaks into C and O ions), each of which can recoil. Any of these reaction products can now deposit energy along their paths by direct ionization. Because these particles are much heavier than the original proton or neutron, they deposit higher charge densities as they travel and therefore may be capable of causing single-event effects. Once a nuclear reaction has occurred, the charge deposition by secondary charged particles is the same as from a directly ionizing heavy ion strike. Recent work has shown that indirect processes can also be important for heavy-ion interactions with high-Z materials [49]. These effects have the most impact on radiation-hardened ICs, and are less important for commercial ICs with low SEU threshold LET that are dominated by direct ionization.

D. Displacement Effects

In addition to ionization effects, high-energy protons, neutrons, and heavy ions can also cause displacement damage in silicon and other semiconductor materials [50]–[52]. As an energetic particle collides with an atom, the

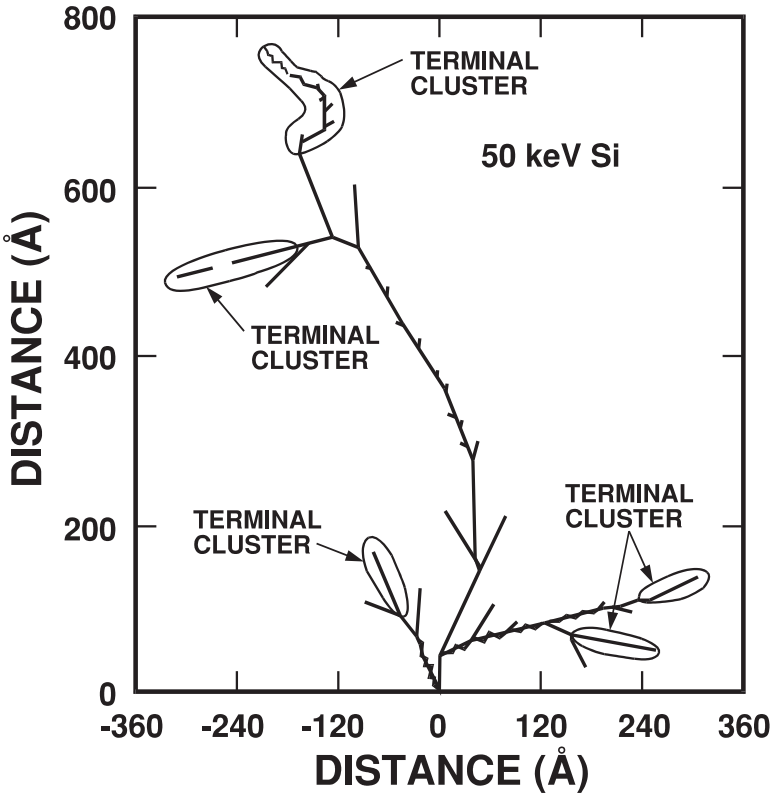

Fig. 18. Defect cascade created by a 50-keV silicon recoil atom. (After Ref. [50])

atom will recoil from its lattice site. If the energy transferred to the atom is high enough, the atom can be knocked free from its lattice site to an interstitial site. The minimum energy required to knock an atom free of its lattice site is called the displacement threshold energy. As the atom is displaced from its original position it leaves behind a vacancy. The combination of the interstitial atom and its vacancy is called a Frenkel pair. If the displaced atom has sufficient energy it can in turn displace other atoms. Thus, for very high energy recoils a defect cascade can be created with large defect clusters. A representative distribution of clusters produced by a 50 keV silicon recoil atom is illustrated in Figure 18 [50]. As the primary silicon atom travels through the silicon, it knocks free other atoms and it is in turn reflected, altering its path. Towards the ends of the paths of the reflected atoms (and the primary atom) large clusters of defects may be formed (terminal clusters). About 90% of the displaced atom and vacancy pairs recombine within a minute after irradiation at room temperature.

The primary effect of displacement damage is the creation of deep and shallow level traps in the material [50]–[52]. The shallow level traps can compensate majority carriers and cause carrier removal. Deep level traps can act as generation, recombination, or trapping centers. These centers can decrease the minority carrier lifetime, increase the thermal generation rate of electron-hole pairs, and reduce the mobility of carriers. As a result, displacement damage is a concern primarily for minority carrier (e.g., bipolar transistors) and optoelectronic devices. It is generally unimportant for MOS transistors except at very high particle fluences.

IV. General Test Considerations

A. Dosimetry

The end result of any hardness assurance test is no more accurate than the accuracy of the dosimetry used for beam analysis. This is true for any type of test. All radiation facilities provide dosimetry for the user. However, users need to be aware that facilities can occasionally (and unintentionally!) provide users with bad information. Two actual cases in point are total dose measurements at a proton facility and SEU measurements at a heavy-ion facility. For the case of the proton facility, the facility operator incorrectly inserted the wrong calibration factor used to measure the proton fluence (off by one decimal place). As a result, devices were irradiated to ten times higher dose than what was intended. This problem was actually discovered during the irradiation when neutron radiation

monitors in the beam room automatically turned the beam off when background neutron levels rose above a set level. Because thermoluminescent dosimeters (TLDs) were periodically used to verify the total dose, this problem would have been eventually detected when the TLDs were read. However, that would have been several days after the testing was completed. For the heavy ion facility case, the facility operator forgot to bias a scintillator plate used to measure the ion fluence. As a result, the ion fluence delivered to the devices under test was approximately ten times too high. This problem was detected by the users recharacterizing the SEU cross section of SRAMs that had been previously characterized at another facility. Even though the operator was originally adamant that the fluence measurements were correct, when presented with the data on the SRAMs the operator took time to diagnose the source of the problem and found the incorrectly-biased scintillator plate.

These examples of faulty dosimetry provided by facility operators illustrate the necessity for the user to have back-up dosimetry or "golden devices" with known radiation response. For example, prior to performing SEU characterizations it is a good practice to first characterize a "golden device" with a known cross section for given test conditions (e.g., ion LET, proton energy, bias supply voltage, memory pattern, etc.). These measurements can also be used to ensure the test equipment is functioning properly. This is especially important when no radiation-induced degradation is observed during qualification testing. Null results may mean the device is very radiation hard, however, they may also suggest that there are problems with dosimetry or the experimental setup (e.g., bad cables, bad power supplies, tester malfunction, etc.).

B. Plotting Results

It is always a good practice to plot data in real time. Experimental problems can often be detected as data is plotted. Plotting data at the facility as it is being collected can save considerable time and expense. For example, as is discussed below, during heavy-ion SEU characterization, the effective LET can be increased by increasing the angle of incidence. However, if the angle of incidence is too high, the sides of the package well can block the beam. This is easily detected by plotting the SEU cross section versus LET. If there is a sudden drop in SEU cross section as the angle of incidence is increased, this is a probable indication that the package well is blocking the beam. Alternatively, plotting maps of the physical location of observed errors can provide a direct indication of beam non-uniformity.

V. Total Ionizing Dose Hardness Assurance Test Issues

A. Total dose hardness assurance test methods

There are a number of qualification test methods that define total-dose testing of microelectronics. These include MIL-STD-883, Test Method (TM) 1019 used in the US and its European counterpart, ESA/SCC Basic Specification (BS) No. 22900. While there are differences between these two test methods, both are intended to provide conservative estimates of the total dose response of microelectronics for use in low-dose-rate applications [53].

Figure 19 shows the main test flow for MOS devices as specified in the latest version of TM 1019 (version 7). This test method is broken into two phases. The first phase of the test method is a conservative test for parametric or functional failure due to radiation-induced oxide-trapped charge buildup in n- and p-channel gate-oxide or parasitic field-oxide transistors. Trapped positive charge in these oxides causes the threshold voltage of n-channel gate and parasitic field oxide transistors to shift toward depletion mode. Large shifts in threshold voltage will cause excessive leakage current to flow from the drain to source of n-channel gate-oxide transistors and can also cause leakage between transistors [54], [55]. In fact, radiation-induced increases in this leakage current limits the radiation hardness of most commercial integrated circuits (ICs). This phase of the test procedure requires an irradiation at $24\pm6^{\circ}$C to a specified dose at a dose rate of 50 to 300 rads(Si)/s using a cobalt-60 gamma ray source followed by a room temperature electrical test ($24\pm6^{\circ}$C). The irradiation and electrical testing is done at $24\pm6^{\circ}$C because radiation effects have been shown to be temperature sensitive [56]–[64]. However, as discussed below, because of this temperature sensitivity electrical characterization testing should also be performed at the temperature extremes of the system environment. During irradiation the devices must be biased using the worst-case bias configuration. This is the bias condition that induces the most radiation induced damage in the device. Worst-case bias conditions are technology dependent and are discussed in detail later in this section. Between irradiation levels, all pins of the device should be shorted together to reduce annealing effects. The time from the end of an irradiation to the

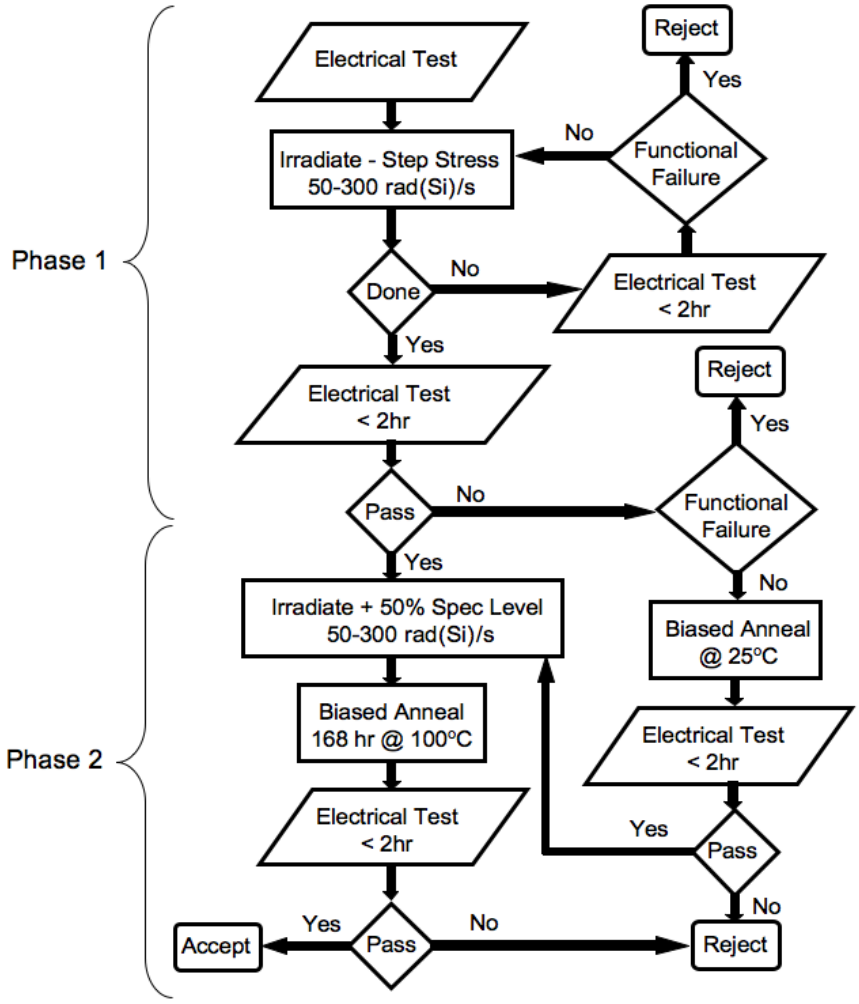

Fig. 19. Test flow for MIL-STD-883, Method 1019.7.

start of electrical testing shall not exceed 1 hour and the start of the next irradiation level must take place within 2 hours of the end of the prior irradiation.

It is important to point out that for some devices in a very low dose rate environment, the first phase of TM 1019 is known to be overly conservative and thus the method allows one to perform extended room temperature anneals to better estimate the performance of devices at low dose rates [65]–[67]. These types of anneals are allowed only for parametric failure (parameters that exceed their specification limit) and not for functional failure. Room temperature anneals are usually effective for devices whose parametric degradation is associated with the buildup of oxide-trapped charge and for devices with fast annealing rates. TM 1019 limits the time for room temperature anneals to the maximum time calculated by dividing the total ionizing dose specification for the devices by the maximum dose rate for the intended use.

In some cases, a second phase (rebound test) of TM 1019 is required. The second phase consists of an additional irradiation equal to 50% of the specified dose, followed by a 168-hour anneal at 100°C under worst-case bias conditions. The additional irradiation is required because of uncertainties in defining the worst-case bias conditions to use during irradiation and anneal [62], [65], [67], [68]. In addition, this overtest is large enough to account for the observed increase in transistor threshold voltage for transistors irradiated at elevated temperatures as opposed to transistors irradiated at room temperature and annealed at 100°C for one week [69]. Typically, irradiations and anneals are performed under static bias conditions, and do not account for the possibility of enhanced rebound voltages often observed during switched-bias or AC irradiations [58], [70]–[72]. After the 1-week anneal, the devices should again be characterized at room temperature. This phase of the test method is used to bound the degradation that is associated with the buildup of interface-trap charge by maximizing the buildup of interface-

trap charge while simultaneously annealing a large amount of oxide-trapped charge. It is a conservative test for parametric or functional failures due to the long-term buildup of interface traps [60], [65]. At the present time, this test is only applied to MOS-like technologies that could exhibit time-dependent effects (TDE), e.g., trapped-hole annealing and interface-trap buildup, over long time periods. A device intended for space application must pass both phases of TM 1019.

BS 22900 has a similar test flow to that of TM 1019. However, there are a few important differences. During the first phase of the test procedure, the irradiations specified by BS 22900 are performed in a range of dose-rate windows, i.e., either between 1 to 10 rads(SiO_2)/s or 0.01 to 0.1 rads(SiO_2)/s at a temperature of 20 ± 10°C with parts biased using worst-case bias conditions. Note that both test methods permit testing to be performed at the dose rate of the intended application if agreed to by the customer. During the second phase of the test procedure, no additional irradiation is required, only biased anneals. The anneals consist of a 24-hour anneal at room temperature followed by a 168-hour anneal at 100°C. Similar to TM 1019, these anneals are used in an effort to account for time-dependent effects in the space environment. The reason no additional dose is required as part of the second phase of BS 22900 is because BS 22900 seeks to accurately identify worst-case conditions during a required evaluation test, which is used during the qualification testing. Electrical testing is performed before and after the irradiations and after the room/elevated temperature anneals at room temperature. A more detailed description of the test philosophy, similarities, and differences between TM 1019 and BS 22900 is given in Ref. [73].

The main test flows of TM 1019 and BS 22900 define test procedures for MOS devices that provide significant insight into device behavior in low-dose-rate space environments. These test procedures were actually developed based on our fundamental understanding of the mechanisms that control radiation effects (as discovered by the mid 80s). However, the 90s led to the discovery of a few new radiation effects phenomena that are not addressed by the main test flow. These include ELDRS in bipolar linear devices and preirradiation elevated temperature effects observed in both MOS and bipolar devices. While the mechanisms that control these effects are not fully understood, there is enough knowledge about the mechanisms to define hardness assurance test procedures, which can assess the impact of these effects. In fact, modifications have been made to TM 1019 to address these relatively new radiation effects. These modifications will be discussed next. In addition, there are a number of issues that can affect the reliability of hardness assurance tests that need to be considered when qualifying devices in space radiation environments. These include selecting the optimum laboratory radiation source, determining worst-case bias conditions, and understanding the implication of characterization temperature. These issues will also be reviewed.

B. Enhanced low-dose-rate sensitivity

Since the early 1990s, it has been known that some types of bipolar devices exhibit enhanced low-dose-rate sensitivity (ELDRS) at low electric fields [74]–[81]. This means that the amount of total dose degradation in bipolar transistors and ICs that is observed at a given total dose is greater at low dose rates than at high dose rates. Note that ELDRS is more than a simple time dependent effect as often observed for MOSFETs. In ELDRS devices, degradation at low-dose rates can be significantly more than at high-dose rates even after taking differences in the time of the irradiations into account, i.e., ELDRS is a "true" dose-rate effect. (This is discussed in more detail below.) In general, total ionizing dose degradation in bipolar devices results from the buildup of radiation-induced charge in the field oxides used to isolate the base and emitter contacts and the creation of recombination centers at the Si/SiO_2 interface. ELDRS in NPN transistors has been attributed primarily to increased positive oxide-trap charge buildup in the isolation oxide overlying the base-emitter junction [80], [82]. This charge enhances the surface recombination rate in the p-base region. On the other hand, lateral and substrate PNP transistors are primarily affected by increased interface-trap charge buildup in the thick isolation oxide over the emitter-base region [79], [83]. In most cases, ELDRS effects have been shown to be more important for lateral or substrate PNP transistors than for NPN transistors [77]. In fact, Johnston and co-workers [77] showed that the relative damage at low dose rates (< 0.01 rad(SiO_2)/s) for junction-isolated linear processes could be greater than a factor of two larger in linear bipolar circuits dominated by PNP transistor response than in those dominated by NPN transistor response. A data compendium of bipolar linear circuits that exhibit ELDRS can be found in Ref. [84].

ELDRS is illustrated in Figure 20, which is a plot of the input bias current (I_{B+}) for LM111 voltage comparators versus total dose for dose rates of 50 and 0.01 rad(SiO_2)/s [81]. The voltage comparators were irradiated and

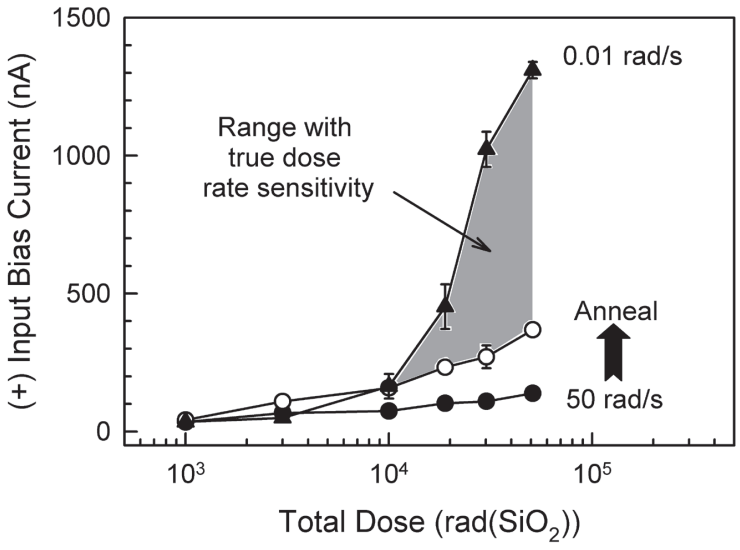

Fig. 20. I_{B+} versus total dose for LM111s subjected to a 175°C, 300-hr preirradiation elevated temperature stress. The devices were irradiated at 0.01 (triangles) and 50 rad(SiO_2)/s (circles) with all pins shorted. Following the 50 rad(SiO_2)/s irradiation, the devices were annealed at room temperature with all pins shorted for a time equivalent to the low dose rate irradiation (open circles). (After [81].)

annealed with all pins shorted. As observed in Figure 20, voltage comparators irradiated at low-dose rates have a much larger increase in input bias current than voltage comparators irradiated at high-dose rates with a room temperature anneal for an equivalent time to the low-dose-rate irradiation time for the same total dose. At dose levels up to 10 krad(SiO_2), there are no "true" dose-rate effects. However, for higher total dose levels, the high-dose-rate irradiation plus room temperature anneal does not degrade I_{B+} nearly as much as the low-dose-rate irradiation. Thus, the difference observed at the higher total dose level (shaded region in the figure) can be attributed to "true" dose-rate effects. This ELDRS effect can cause failure of ICs in satellite environments not observed in standard laboratory testing. As such, ELDRS severely complicates hardness assurance testing for space environments.

Developing an accelerated hardness assurance test method to estimate the "true" low-dose-rate effects in bipolar devices remains a very challenging issue facing the radiation effects community [85], [86]. Unfortunately, high-dose-rate irradiation followed by room temperature annealing, which can often accurately estimate the radiation response of CMOS devices at low dose rates [60], [62], does not accurately estimate the low-dose-rate response of many types of bipolar devices [74], [78], [81]. CMOS devices generally exhibit time-dependent effects rather than "true" dose-rate effects. Time-dependent effects can also exist in bipolar devices and must not be confused with true dose-rate effects. "True" dose-rate effects make it difficult to develop quick and accurate total-dose hardness assurance test methods for predicting the radiation response of bipolar devices. Currently, the most promising rapid screen involves the use of elevated temperature irradiations at relatively low dose rates ($\leq$1 rad(SiO_2)/s) [87]–[89]. However, the optimum irradiation temperature for this procedure varies from technology to technology [84], [88], does not always bound the low-dose-rate response, and the required dose rate is significantly lower than the current dose rate range (50 to 300 rad(SiO_2)/s) normally used for qualifying CMOS technologies. In addition, it has recently been suggested that if the radiation-induced charge that is responsible for ELDRS (whether it be interface or border traps) can anneal at 100°C, then elevated temperature irradiations may also cause some annealing of radiation-induced charge [90]. This is consistent with previous data on MOS devices that show some interface-trap annealing at radiation temperatures above 90°C [91]. These data help explain why high-dose-rate irradiations at elevated temperatures, in some cases, underestimate low-dose-rate degradation. Whether this occurs likely depends on the rate-limiting mechanisms of hydrogen interactions (i.e., passivation and depassivation of interface traps) at the silicon/silicon dioxide interface [92]. As a result, manufacturers do not have a reliable laboratory test guideline for timely assessment of the radiation hardness of their bipolar technologies. Nevertheless, irradiating at elevated temperature is allowed by TM 1019 if characterization testing shows that this procedure can bound the low-dose rate induced degradation for bipolar, BiCMOS, or mixed-signal devices. Without prior characterization testing, the

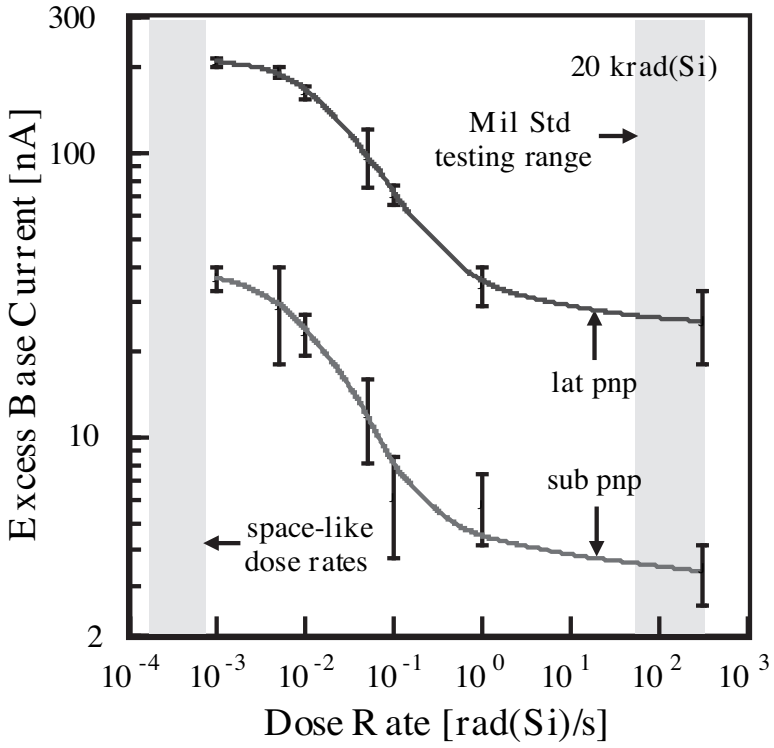

Fig. 21. Effect of dose rate on excess base current in the lateral and substrate PNP bipolar transistors. All data were measured at V_{EB} = 0.7 V. (After [93].)

only test procedure for ELDRS that is currently allowed by TM 1019, requires that parts be irradiated at dose rates of $\leq$ 10 mrad(SiO_2)/s. For most devices the amount of enhanced degradation has been observed to saturate at these dose rates. This is shown in Figure 21 [93]. This figure shows the effect of dose rate on excess base current in lateral and substrate PNP bipolar transistors. The amount of degradation for both lateral PNP and substrate PNP transistors begins to saturate at dose rates below approximately 10 mrad(SiO_2)/s. Of course, there are always exceptions to this general observation. Johnston et al. [87] showed enhanced degradation between 5 mrad(SiO_2)/s and 2 mrad(SiO_2)/s for a LM324 op-amp manufactured by Motorola. However, this is the only known part to exhibit this behavior.

On a positive note, researchers have recently shown that by changing the final chip passivation layers it is possible to significantly reduce or eliminate ELDRS in some bipolar linear technologies [94]–[97]. It has been shown that devices fabricated without passivation layers do not exhibit ELDRS or pre-irradiation elevated temperature stress (PETS) sensitivity (discussed in detail next), while devices from the same production lot fabricated with other passivation layers are ELDRS and PETS sensitive. It has also been shown that removing the passivation layers on devices that exhibit ELDRS could mitigate ELDRS and PETS effects, as illustrated in Figure 22 [94]. While this is obviously not a practical solution to the ELDRS and PETS problems for ICs to be used in space systems, it does appear to indicate that ELDRS and PETS effects are probably not intrinsic to many bipolar process technologies prior to deposition of the final passivation layer. In addition, ELDRS and PETS effects do not appear to be inherently related to circuit design or layout, but are related to mechanical stress effects, hydrogen in the device, or a combination of the two. It appears that mechanical stress induced by the passivation layers might play a critical role in determining the radiation response of bipolar linear ICs. Passivation layers can easily alter mechanical stress in the die. The introduction of thermal cycles and moisture after fabrication have been shown to further impact the film stress [98], [99]. These two facts are consistent with both changes in radiation response between unpassivated and passivated devices at high-dose rates, and the observation of PETS sensitivity in passivated devices. These results suggest that proper engineering of the final chip passivation layer might eliminate ELDRS and PETS effects in bipolar integrated circuits. In addition, it has recently been shown that hydrogen introduced during the packaging cycle can have an impact on the radiation response of bipolar linear devices that exhibit ELDRS [100]. As a result,

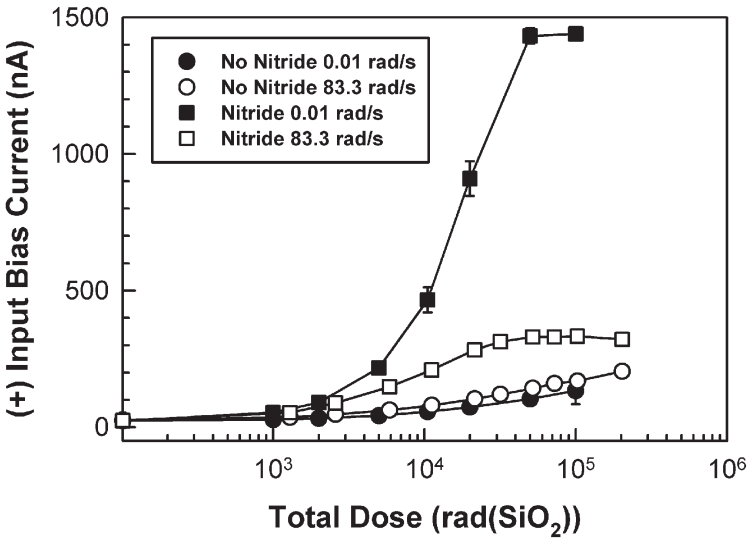

Fig. 22. I_{B+} versus total dose for LM111s with and without the nitride passivation layer removed, irradiated at 0.01 or 83.3 rad(SiO_2)/s with all pins shorted. (After [94].)

it is recommended that all hardness assurance testing be conducted on devices in their final package configuration.

C. Preirradiation elevated temperature stress (burn-in) effect

ICs are exposed to numerous thermal cycles (e.g., during packaging, reliability testing, system assembly and system use) during their life time and prior to their exposure to radiation. It has been shown that these preirradiation elevated temperature stresses (PETS) can dramatically change the total dose radiation response of both MOS [101]–[104] and bipolar [105], [106] devices. Examples of the effects of preirradiation elevated temperature anneals are shown in Figures 23 and 24 [101], which are plots of the threshold-voltage shift for MOS gate-oxide (Figure 23) and field-oxide (Figure 24) transistors versus total dose. Transistors with and without a preirradiation 150°C, one-week anneal (typical burn-in conditions) were irradiated with 10-keV x rays with a 5-V gate-to-source bias. At the higher radiation levels, both the gate-oxide and field-oxide threshold-voltage shifts were larger for the transistors subjected to the preirradiation elevated temperature anneal. The larger threshold-voltage shifts for the transistors subjected to a preirradiation anneal could be due to either an increase in radiation-induced oxide-trap charge, a decrease in interface-trap charge, or both. Based on charge-separation measurements [101], [102], it was shown that for these devices the major cause for the larger threshold-voltage shifts for the devices subjected to a preirradiation anneal was less radiation-induced interface-trap buildup in gate oxides and more radiation-induced oxide-trapped charge buildup in field oxides. These changes in radiation-induced charge buildup have been shown to lead to larger increases in IC static power supply leakage current during irradiation, and to a lesser degree increases in timing parameters. The functionality of the devices can also be impacted. In addition, It has been shown that some linear bipolar technologies are also sensitive to PETS [105], [106]. The mechanisms for the PETS effect for linear bipolar technologies appear to be qualitatively similar to those for CMOS technologies.

Note that not all technologies exhibit a PETS effect. However, for those technologies that do, the magnitude of the PETS effect can be affected by the time and temperature of the preirradiation elevated temperature stress but appears to be independent of the PETS bias condition [102]. The effects of time are illustrated in Figure 25 for 3.3-V Paradigm SRAMs [103]. Figure 25 is a plot of the increase in word (or byte) failure count as a function of total dose for a complement checkerboard pattern written to the SRAMs. Data for SRAMs with no stress or a 24-, 336-, 672-, and 802-hour pre-irradiation 150°C stress with nominal values of V_{DD} applied during the elevated temperature biased stress are shown. The SRAMs were irradiated using a Co-60 source in steps up to 100 krad(SiO_2) at a dose rate of 64.5 rad(SiO_2)/s. As the pre-irradiation stress time increases, the word failure count curves shift to lower doses. These data suggest that the PETS effect is associated with a thermally activated process. It has

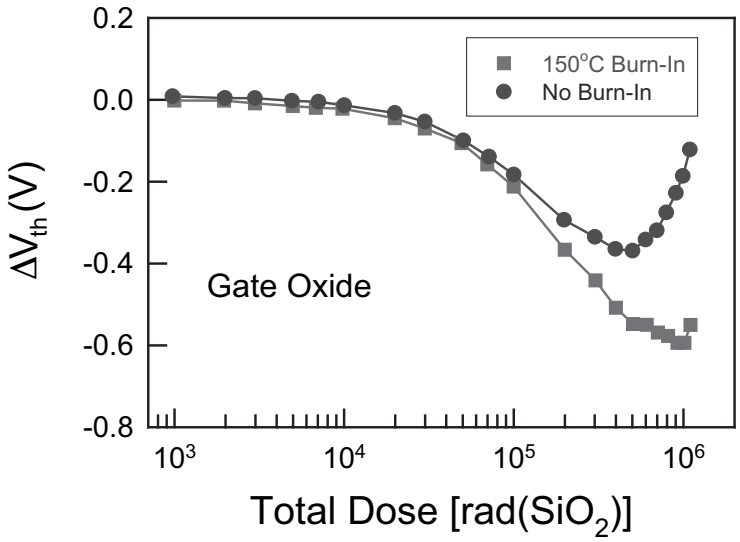

Fig. 23. Threshold-voltage shift versus total dose for gate oxide n-channel transistors with and without a PETS irradiated with a 10 keV x-ray source with a 5 V gate-to-source bias. The PETS was for one week at a temperature of 150°C. (After [101].)

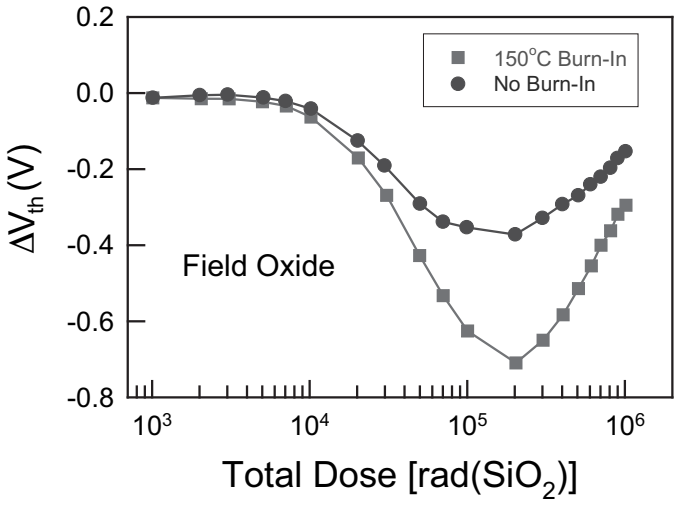

Fig. 24. Threshold-voltage shift versus total dose for field oxide n-channel transistors with and without a PETS irradiated with a 10-keV x-ray source with a 5-V gate-to-source bias. The PETS was for one week at a temperature of 150°C. (After [101].)

been found that the activation energy is 0.38 eV [102]. This activation energy is close to the activation energy of 0.41 eV for trapped hole compensation [60] and the activation energy of 0.45 eV for the diffusion of molecular hydrogen in bulk fused silica [107]. The latter suggests that the PETS effect may be related to the diffusion of molecular hydrogen. The lack of a strong bias dependence is consistent with this mechanism. The preirradiation stress could also affect the spatial and energy distribution of hole-trap precursors in the oxide (this may also involve the diffusion of hydrogen related species), leading to differences in trapped-hole distributions following irradiation. Clearly, more work needs to be performed to conclusively identify the mechanisms for the PETS effect.

The effect of preirradiation elevated temperature stresses on IC radiation response is clearly a concern for hardness assurance testing. The U. S. military test guideline TM 1019 has been modified to address PETS effects as illustrated in Figure 26. Before the modification, the test guideline permitted manufacturers to qualify the total-dose radiation response prior to elevated temperature reliability screens. This raised the possibility that the total-dose radiation

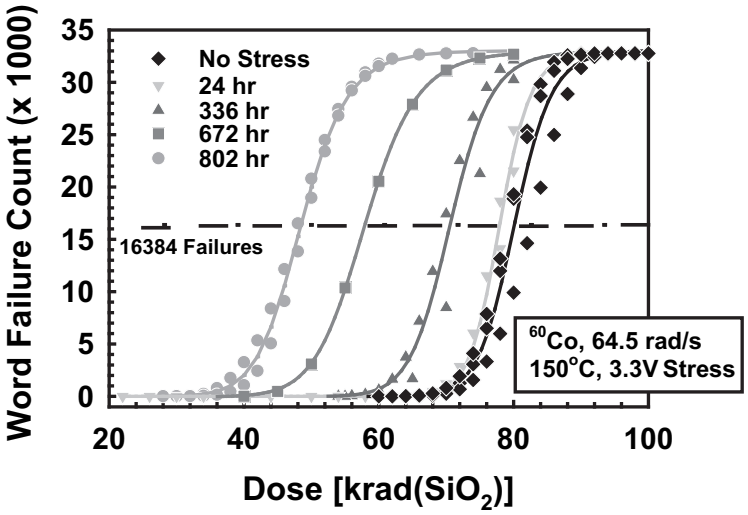

Fig. 25. Increase in the word failure count for a checkerboard pattern written to 3.3-V Paradigm SRAMs versus dose for SRAMs with no pre-irradiation stress or various pre-irradiation stresses up to 35 days at 150°C. (After [103].)

response of ICs sensitive to PETS effects could be significantly different than the radiation response of ICs used for qualification testing. Thus, TM 1019 was modified to require manufacturers to perform radiation qualification testing on ICs after burn-in. Unless it has been shown by prior characterization or by design that burn-in has negligible effect on total dose radiation-induced degradation, radiation testing must be performed after subjecting parts to burn-in or the manufacturer must develop a correction factor that accounts for changes in total dose response resulting from subjecting product to burn-in. While these changes to TM 1019 are a step in the right direction, they may underestimate the radiation response of PETS sensitive devices at the end-of-life of system use [103]. As noted above, the PETS effect appears to be associated with a thermally activated process. Thus, as PETS sensitive devices continue to be exposed to thermal cycles during system assembly, one would expect that the total dose response of the devices could continue to degrade. Thus, the estimated degradation measured on devices after burn-in, as required by TM 1019, may not be a conservative estimate of the worst-case degradation observed at the end-of-life. To determine the response of PETS sensitive devices at the end of life, one would need to account for all thermal cycles that the device is exposed to after burn-in, including thermal cycles that the devices are exposed to during system assembly and use [103]. Otherwise, the amount of radiation-induced degradation may be severely underestimated.

D. Optimum laboratory radiation sources for hardness assurance testing

Total-dose degradation of electronic devices used in space is caused primarily by exposure to high fluences of electrons and protons. However, Co-60 gamma and x-ray sources are more cost effective for routine evaluation of the radiation hardness of electronic devices for these applications. In this section, we will review which of these two sources are best suited for simulating energetic electrons or protons. X-ray sources can operate at higher dose rates than most Co-60 sources and can be used to irradiate individual die at the wafer level. Because of these properties, x-ray sources are often used for process development and control [108], while Co-60 gamma sources are normally used for hardness assurance testing [62]. The justification for using Co-60 gamma sources for hardness assurance testing is based primarily on historical practice rather than on technical grounds. Some work has been performed comparing the differences in total-dose degradation for x-ray and Co-60 irradiations. In some cases, good correlation between Co-60 and x-ray radiation-induced degradation was observed [109]; however, in other cases large differences were observed [67], [110]. Thus, it is important to determine which radiation source is best suited for simulating energetic electrons or protons. Recent work [111] comparing the radiation-induced response of pMOSFET dosimeters showed that the radiation-induced response for high-energy protons (60 to 200 MeV) was

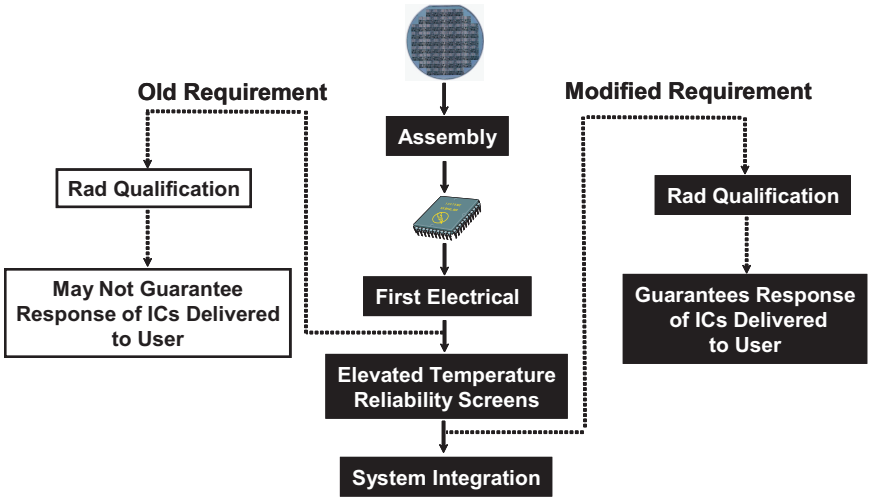

Fig. 26. Modifications made to MIL-STD-883, TM 1019 to account for PETS effects. (After [103].)

only 65-85% of the Co-60 radiation-induced response. This result raises concern that Co-60 radiation sources may not be the best radiation source for simulating device response in proton-rich space environments.

To understand why there might be differences in the radiation-induced degradation in devices irradiated with Co-60 or x-ray irradiation, one must examine the differences in charge yield between the sources. If an electric field exists across the oxide of an MOS transistor, once released, electrons in the conduction band and holes in the valence band will immediately begin to transport in opposite directions. Electrons are extremely mobile in silicon dioxide and are normally swept out of the silicon dioxide in picoseconds [112], [113]. However, even before the electrons can leave the oxide, some fraction of the electrons will recombine with holes in the oxide valence band. This is referred to as initial recombination. The fraction of holes that do not recombine is referred to as the charge yield. The amount of initial recombination is highly dependent on the electric field in the oxide and the energy and type of incident particle [114], [115]. In general, strongly ionizing particles form dense columns of charge where the recombination rate is relatively high. On the other hand, weakly ionizing particles generate relatively isolated charge pairs, and the recombination rate is lower [114]. Figure 27 is a plot of the fraction of unrecombined holes (charge yield) versus electric field for Co-60 and x-ray irradiations [115]. The plot shows that there can be significant differences in the charge yield between the two sources. In fact, at low fields the relative difference can be very large ($>$50%). Thus, the laboratory radiation source, x-ray or Co-60, that best matches proton or electron radiation-induced degradation in space may depend on which source gives the best match in charge yield.

Unfortunately, there is presently limited data in the literature for the charge yield of electrons and protons for the energy range of these particles in space [116]. To gain insight into which laboratory radiation source gives the best match in charge yield to electrons and protons, one can examine the stopping power for electrons and protons in SiO_2. Figure 28 is a plot of the stopping power in SiO_2 for electrons and protons versus particle energy [117]. The energy range shown for protons and electrons covers that typically found in space [118]. Also shown in the figure are the calculated average values of stopping power for secondary electrons generated by 10-keV x rays and 1.25-MeV Co-60 gamma rays. These values are based on calculations using the Sandia radiation transport code CEPXS/ONELD [119]. The interaction of a 10-keV photon and a 1.25-MeV photon with a thin layer of SiO_2 produces a secondary electron spectrum with an average energy of 5.5 keV and 590 keV, respectively. The stopping power of the electrons generated by a 10-keV photon more closely matches the stopping power of the lower energy protons (20 to 60 MeV) than the stopping power of electrons generated by a 1.25-MeV photon. On the other hand, the stopping power of the electrons generated by a Co-60 photon more closely matches the stopping power of the electrons in space (up to 7 MeV) [118].

As a result, we can expect that for low energy protons, the charge yield of the protons is more closely matched by the charge yield of the secondary electrons generated by a 10-keV photon (x-ray) than the secondary electrons generated by a 1.25-MeV photon (Co-60 gamma). This suggests that, at least for lower energy protons, a 10-keV x-ray source may better simulate the radiation-induced degradation caused by protons than a Co-60 radiation source.

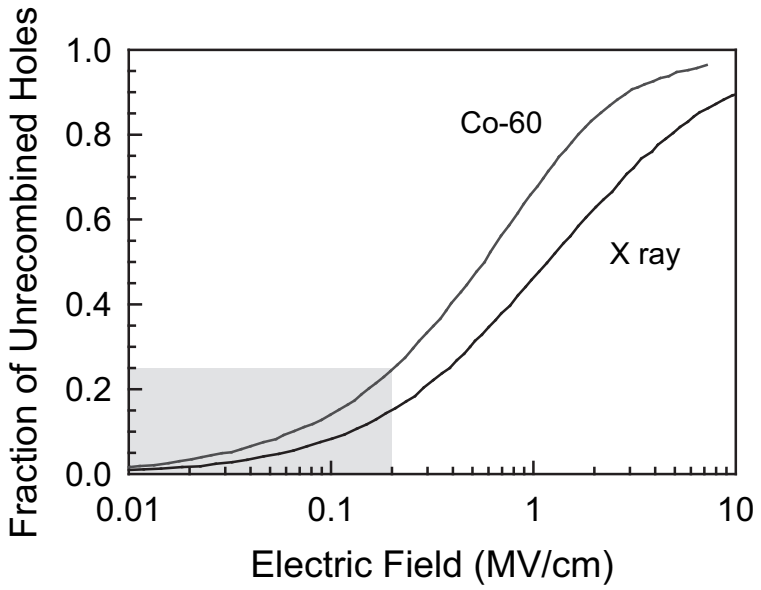

Fig. 27. Fraction of holes that escape recombination for 10-keV x-ray and Co-60 irradiations as a function of oxide field. (After [115].)

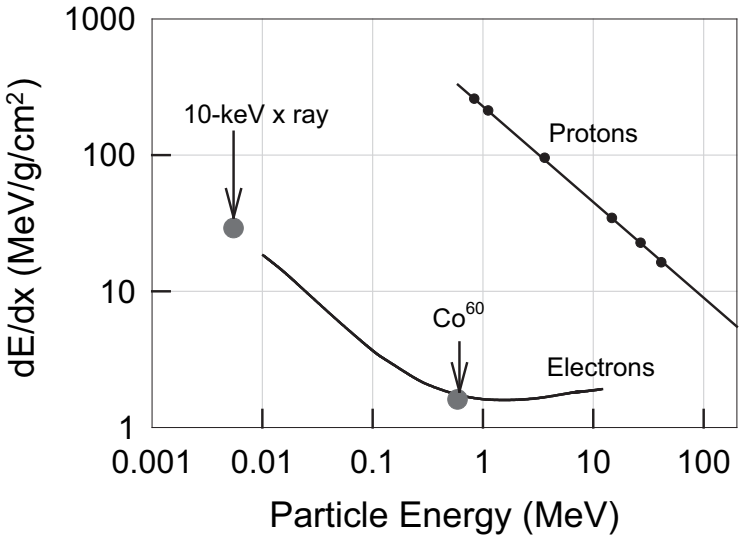

Fig. 28. Stopping power versus particle energy for electrons and protons. Also shown are the average stopping powers for secondary electrons emitted by 10-keV x rays and 1.2-MeV gamma rays. (After [117].)

This was indeed found to be the case [120]. Figure 29 shows the ratio of the back-gate transistor threshold-voltage shift for x-ray and proton irradiations and the ratio for Co-60 gamma and proton irradiations for SOI transistors irradiated in the 0 V and transmission-gate (TG) bias configurations. The x-ray and proton data were taken at a dose rate of 270 rad(SiO_2)/s and the Co-60 gamma data were taken at a dose rate of 50 rad(SiO_2)/s. X-ray data taken at 270 and 50 rad(SiO_2)/s showed no noticeable differences in back-gate threshold-voltage shift for the different dose rates for devices irradiated to total doses up to 500 krad(SiO_2). Hence, the fact that the data were taken at somewhat different dose rates should not affect the conclusions. Within experimental uncertainties, the x-ray and proton radiation-induced back-gate threshold-voltage shifts are nearly equal for all total dose levels and bias conditions examined. However, the ratio of Co-60 gamma and proton back-gate threshold shifts varies widely, especially for low total doses. The fact that there is agreement in the back-gate threshold-voltage shifts at high total doses is not surprising. At this point, the threshold-voltage shift is significant and therefore the internal field in the

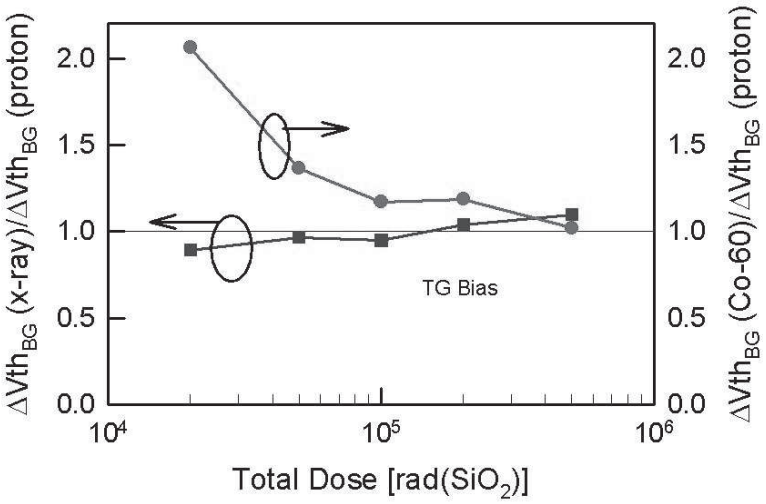

Fig. 29. Ratio of x-ray to 41.4-MeV proton and Co-60 gamma to 41.4-MeV proton radiation-induced back-gate threshold-voltage shifts as a function of total dose for SOI transistors. Transistors were irradiated with either a 0 V or TG bias configuration. (After Ref. [120].)

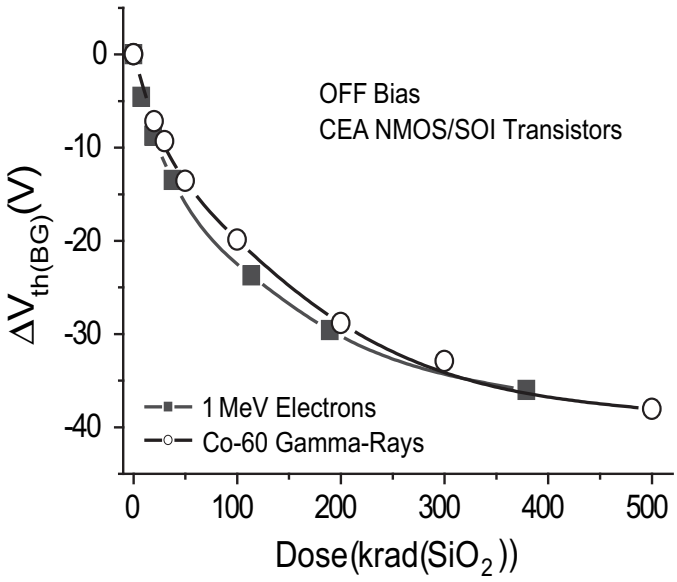

Fig. 30. Back-gate transistor threshold voltage shift versus total dose for CEA SOI transistors irradiated with Co-60 gamma rays and 1-MeV electrons with the OFF bias configuration. (After [116].)

oxide is also significant. Thus, a low field condition in the oxide is no longer satisfied. Note that this is due to the size of the threshold voltage shift in these devices, not the total dose. Devices that shift more or less with dose will therefore reach this point at different dose levels. For this proton energy, these total dose levels, and these devices, x-ray irradiations simulate proton radiation-induced degradation much better than Co-60 gamma irradiations. Good correlation between x-ray and proton radiation-induced degradation has been observed for proton energies between 20 and 200 MeV and also in the radiation-induced degradation of field oxides in bulk-silicon technologies [120].

The flux of electrons and protons in space varies widely with orbit altitude and inclination. For example, for low earth orbits (especially for orbits passing through the South Atlantic Anomaly), the proton flux can be very high compared to the electron flux. In contrast, for higher orbits, the proton flux can be very low in comparison to the electron flux [118]. Based on the results of Schwank et al. [120], for SOI and bulk-silicon transistors, laboratory x-ray irradiations may more closely simulate proton-rich environments such as low-earth orbits (at least in the energy range of 20 to 200 MeV) than laboratory Co-60 gamma irradiations. This contradicts the commonly accepted tenet that Co-60 gamma sources should be used for all hardness assurance qualification. As previously discussed, the

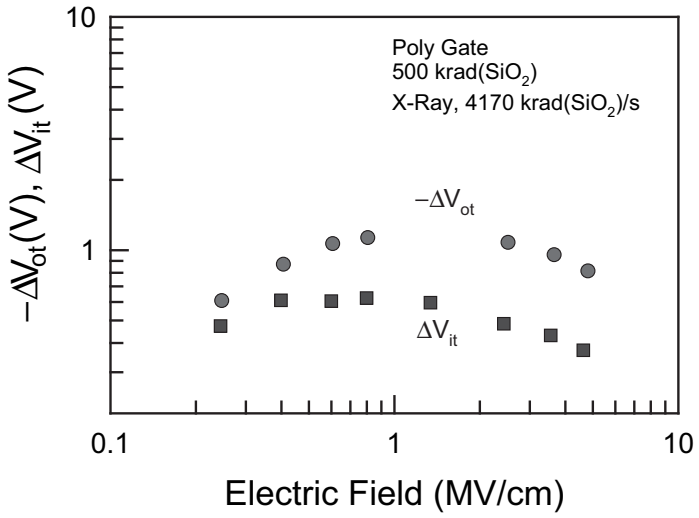

Fig. 31. Voltage shift due to oxide and interface-trap charge versus electric field for n-channel transistors with 45 nm oxides irradiated to 500 krad(SiO_2). (After [121].)

better match between x-ray and proton radiation-induced damage is likely due to a closer match of the initial charge yield at low electric fields. However, this does not preclude the use of Co-60 gamma radiation sources for device qualification in proton-rich environments. Co-60 gamma radiation sources may overestimate the total dose degradation and, therefore, are a more conservative radiation source. In contrast, we note from Figure 28 that Co-60 gamma irradiation more closely matches the stopping power (and hence, the charge yield) of electrons than x-ray irradiation. Thus, to simulate total dose degradation in electron-rich environments such as geosynchronous orbits, Co-60 gamma sources are probably still the optimum laboratory radiation source for device qualification, as shown in Figure 30 [116]. Figure 30 is a plot of the back-gate threshold voltage shift versus total dose for transistors irradiated to total doses up to 500 krad(SiO_2) with Co-60 gamma rays and 1 MeV electrons in the OFF bias configuration. The 1-MeV electron data are in very good agreement with the Co-60 data; the differences are within experimental uncertainties due to errors in dosimetry or to part-to-part variations. This observation is consistent with the similarity observed between the charge yield of Co-60 gammas and 1-MeV electrons in thermal gate oxides as discussed above.

E. Worst-case bias

The worst-case radiation and anneal bias conditions for ICs should be determined through an analysis of the system application and characterization testing. As will be discussed below, the worst-case bias condition will depend on the failure mechanism(s), which can vary as a function of circuit parameters, dose rate, and temperature. As a result, characterization testing should be done over the full range of system operating conditions.

1) Si bulk devices: It is well known that bias conditions can have a large effect on the amount of radiation-induced degradation. For gate oxides, the maximum threshold-voltage shift for oxide-trap and interface-trap charge occurs at intermediate values of electric field. This is illustrated in Figure 31, which is a plot of the measured radiation induced voltage shift due to oxide and interface-trap charge for polysilicon gate transistors irradiated to 500 krad(SiO_2) [121]. At high electric fields, the threshold-voltage shifts due to oxide-trap and interface-trap charge decrease with increasing electric field strength because the capture cross section for holes decreases with increasing electric field [122]–[126]. At low electric fields, the threshold-voltage shifts due to oxide-trap and interface-trap charge are small because the number of radiation-induced electron/hole pairs which escape initial recombination (charge yield) is small (see Figure 27). Thus, the maximum threshold-voltage shifts due to oxide-trap and interface-trap charge occur at moderate electric fields (1 to 2 MV/cm).

For advanced IC technologies with very thin gate oxides ($<$10 nm), radiation-induced oxide-trapped charge buildup in field oxides and in SOI buried oxides normally dominates the radiation-induced degradation of ICs. The

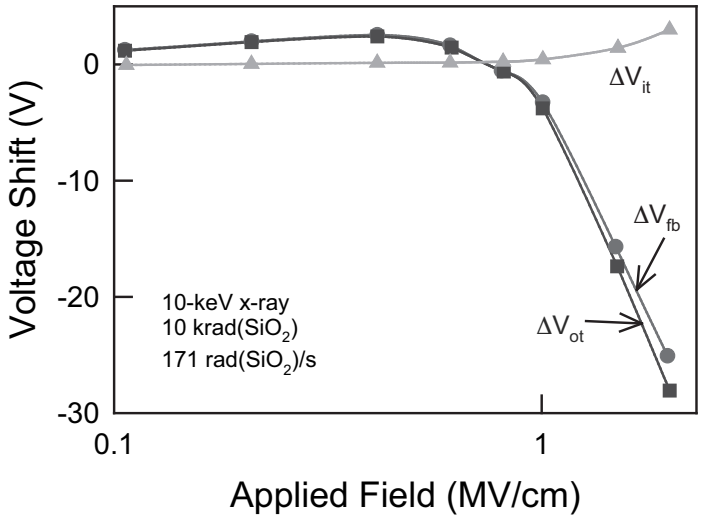

Fig. 32. Flatband voltage shift and the threshold-voltage shift due to oxide and interface-trap charge versus applied field during x-ray irradiation for capacitors fabricated using a traditional field oxide insulator as the gate dielectric. (After [55].)

worst-case bias for parasitic field oxide leakage current is the highest operating voltage of the technology. The worst-case bias condition for radiation-induced charge buildup in field oxides is the bias condition that maximizes the electric field across the field oxide. This is clearly shown in Figure 32, which is a plot of the flatband, oxide-trap charge, and interface-trap charge voltage shifts versus applied field for capacitors irradiated with 10-keV x rays to a total dose of 10 krad(SiO_2) [55]. The capacitors were fabricated using a traditional field oxide as the gate dielectric. The dielectric was deposited using a traditional shallow-trench isolation (STI) process. For these bias and irradiation conditions, there is no significant buildup of interface-trap charge in the field oxide. However, at high electric fields, there is a very large radiation-induced buildup of oxide-trapped charge, which causes a very large threshold-voltage shift of the field oxide transistor. After irradiation, the threshold-voltage shift was greater than 25 V for electric fields greater than 2 MV/cm. Depending on the initial threshold voltage of the field oxide transistor, this radiation-induced threshold-voltage shift may be large enough to cause large increases in transistor leakage current.

While the electric fields across the majority of field oxides are generally very low for most advanced technologies having operating voltages less than 5 V, this is not the case for all areas of the field oxides. For example, very high electric fields can occur at the corners of STI oxides, as illustrated in Figure 33 [55]. In this figure, simulations show that the electric field can be as high as $\sim$6 MV/cm at the Si corner of the n+ region (source/drain region of an n-channel gate oxide transistor). Although the electric field decreases rapidly with distance from the trench corner (down the trench sidewall or into the trench region), the electric field still remains relatively high ($>$1 MV/cm) for the first 20 nm. Thus, the bias condition that will result in the maximum electric field across the STI is the bias condition that gives the maximum voltage drop between the gate and the substrate. This bias condition is normally the ON bias condition, where the gate is at the bias supply voltage, V_{DD}, and the source, drain, and substrate are grounded. Although these results were demonstrated for STI, similar results are obtained for ICs with LOCOS isolation.

Conceptually, selecting a worst-case bias for bulk-silicon ICs can be difficult because the worst-case bias for gate and field oxides may be different. However, for advanced technologies where the irradiation response is dominated by radiation-induced parasitic leakage current, the optimum worst-case bias for an IC is that which maximizes parasitic field oxide leakage, i.e., the maximum operating voltage. Ideally, an IC should be irradiated in the state that produces the most radiation-induced degradation and the IC should be tested post-irradiation in the condition that shows the most electrical degradation. For example, a transistor can be irradiated in the ON state to produce the largest radiation-induced leakage current and measured in its lowest current state (the OFF state), which will show the largest increase in leakage current. Similarly, to observe the largest increase in current in an SRAM, one

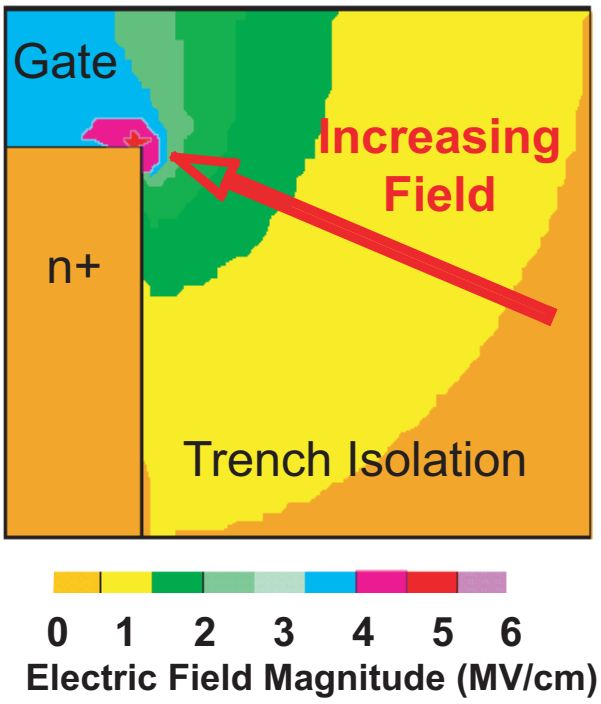

Fig. 33. The cross sections illustrate the electric field magnitude near the corner of the shallow-trench isolation for the case in which the trench insulator is planar with the 13-nm gate oxide. Electrostatic potential in the trench region was simulated with the polysilicon gate that extends over the STI (not shown) biased at 5 V and all other regions grounded. (After [55].)

often irradiates the IC in a checkerboard pattern and then measures the IC leakage current post-irradiation in the complement checkerboard pattern [101], [108], [127].

2) SOI devices: Worst case bias conditions for SOI devices can be more difficult to determine than for bulk Si devices. For SOI devices, the radiation response is controlled by charge buildup in the SOI buried oxides in addition to charge buildup in the gate and field oxides. Similar to field oxides as discussed above, the buildup of radiation-induced charge in SOI buried oxides is dominated by positive oxide-trapped charge. Therefore, the electric field condition that results in the maximum back-gate threshold-voltage shift in an SOI transistor is the bias condition that causes the most radiation-induced hole trapping near the back Si/SiO_2 interface. This will be the bias condition that results in the maximum electric field strength in the buried oxide underneath the channel region. For typical gate lengths and buried oxide thicknesses, the bias condition that produces the largest electric fields underneath the channel and the most hole trapping is the transmission gate bias configuration for partially-depleted transistors. The transmission gate (TG) bias configuration is defined as source and drain biased at V_{DD}, while the gate and body contacts (if available) are grounded. Simulations and data [128] have also shown that the OFF bias condition (drain at V_{DD} and all other contacts grounded) can result in very large back-gate threshold-voltage shifts. The bias configuration that results in the largest back-gate threshold-voltage shifts depends on the ratio of the transistor gate length and the buried oxide thickness [128]. These simulations have been experimentally verified [110], [128], [129]. Figure 34 is a plot of the measured back-gate threshold-voltage shifts versus gate length for partially-depleted n-channel SOI transistors irradiated with 10-keV x rays to a total dose of 1 Mrad(SiO_2) [128]. The buried oxide thickness was 413 nm. The largest back-gate threshold-voltage shifts observed were in transistors irradiated in the TG bias configuration. However, for transistors with gate lengths near the standard technology gate length of 0.25 μm, the back-gate threshold-voltage shifts were approximately the same for transistors irradiated in the TG and OFF bias configurations. The smallest back-gate threshold-voltage shifts were for transistors irradiated in the ON bias configuration. These results for the worst-case bias configuration for partially-depleted SOI transistors are just the opposite of that for the worst-case bias configuration for radiation-induced charge buildup in field oxides discussed above.

For fully-depleted SOI transistors, the worst-case bias is not as well defined as for partially-depleted SOI transistors. Similar to the case for partially-depleted SOI transistors, Jenkins and Liu [130] showed that for some

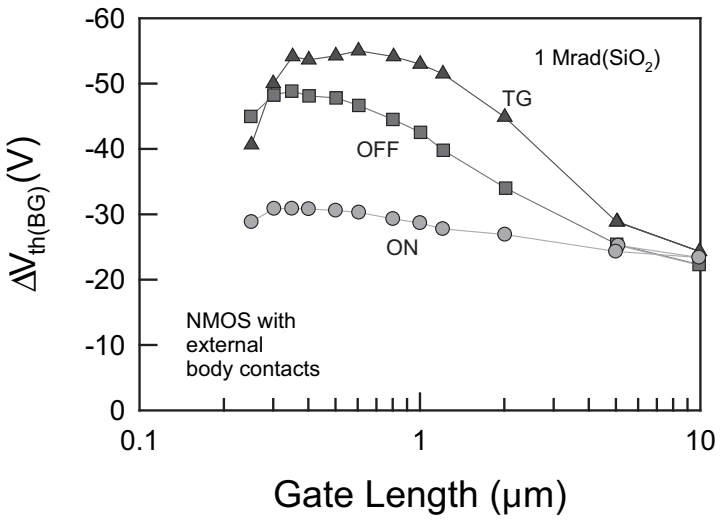

Fig. 34. Back-gate threshold-voltage shift versus gate length for an n-channel partially-depleted SOI transistor irradiated with x rays to a total dose of 1 Mrad(SiO_2). Transistors were biased in the ON, OFF, and TG bias configurations. (After [128].)

SOI technologies, the worst-case bias for radiation-induced charge trapping in the buried oxide was the transmission gate bias configuration. However, for other technologies, the worst-case bias was determined to be the ON bias configuration [131].

Because the worst-case bias configuration for radiation-induced charge buildup in field oxides and SOI buried oxides may be different, hardness assurance testing of SOI devices can be difficult. Both parasitic field oxide leakage and transistor leakage induced by radiation-induced charge trapping in the buried oxide can be very large. Thus, both must be accounted for. This is especially important when estimating IC hardness from transistor testing. Both radiation-induced field oxide and buried oxide leakage will contribute to the leakage current of gate-oxide transistors. Radiation-induced field oxide leakage will also contribute to the leakage current of the back-gate transistor. To ensure worst-case conditions are satisfied, SOI transistors should be irradiated in the ON and TG or OFF bias configurations. For ICs, the different worst-case bias configuration is less problematic. For instance, regardless of the input bias conditions, in an SRAM approximately half of the transistors will be irradiated in the ON bias configuration and the other half will be irradiated in the OFF bias configuration. Some transistors will also be irradiated in the TG bias configuration. Therefore, worst-case bias conditions in an SRAM are automatically probed using standard input bias conditions. However, for SOI circuit types where the number of OFF (or TG) and ON biased transistors can be considerably different, ICs may require testing in multiple bias configurations to ensure worst-case conditions are satisfied.

3) Bipolar devices: In contrast to MOS devices in which the worst-case bias condition is typically a DC bias condition at the maximum operating voltage of the device, the worst-case bias condition for some bipolar devices can actually occur at low electric fields. Specifically, this applies to bipolar devices that exhibit ELDRS, where the amount of degradation was observed to be maximum at low bias levels (i.e., all pins grounded) [80]. The worst-case bias condition for a bipolar IC that exhibits ELDRS will depend on the circuit parameter that is most sensitive to low-dose-rate irradiation. In general, the worst-case bias condition for changes in input bias current of a bipolar linear IC is all pins grounded; whereas the worst-case bias condition for changes in offset voltage is for devices biased in a DC bias condition. While these are general observations, it is a good practice to do characterization testing to determine the worst-case radiation bias conditions for ICs before performing qualification testing.

F. Implication of characterization temperature

This final subsection addresses an emerging total dose hardness assurance issue. Specifically, it addresses the potential need to characterize ICs over the full system temperature range before and after irradiation to ensure system functionality. While the community as a whole has not yet agreed to make any changes to the existing

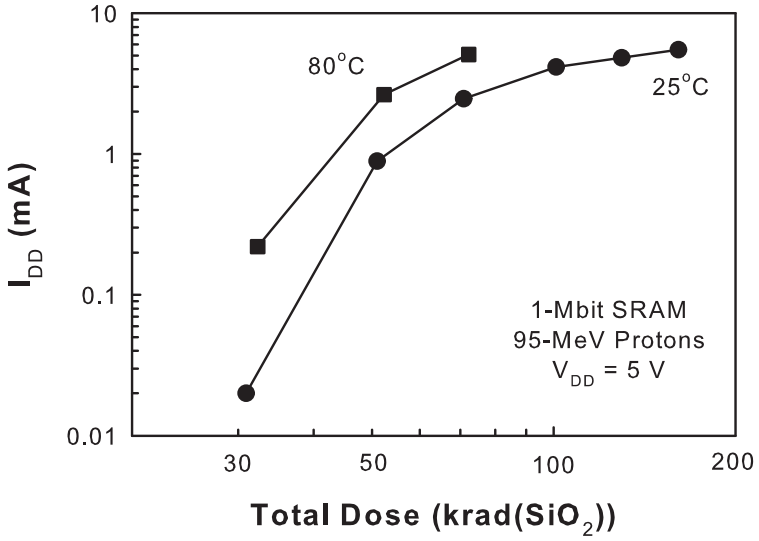

Fig. 35. Static supply leakage current versus temperature for 1-Mbit SRAMs irradiated with 95-MeV protons at a dose rate of 17 rad(SiO_2)/s at room temperature (25°C) with V_{DD} = 5 V and characterized at room temperature and 80°C. (After [136].)

total dose test methods to require characterization testing over the full system temperature range, it is important to discuss this emerging issue and to discuss potential test method modifications that could be made to address this issue.

ICs are often required to operate over a wide range of temperatures in many system applications. For example, military hardened devices are often specified to operate from -55°C to 125°C, whereas COTS devices might be required to operate over a smaller temperature range, e.g., -40°C to 85°C. It is well known that device characteristics are impacted by operation temperature. Whatever the temperature range specified, manufacturers typically guarantee that their devices will operate within limits specified in the product specification over this temperature range. The manufacturer establishes these limits by routinely characterizing devices as a function of temperature before irradiation. However, the same device characteristics affected by operation temperature (e.g., threshold voltages, leakage currents, and carrier mobilities) are also affected by ionizing radiation. [108], [127], [132]–[135]. Unfortunately, because the annealing of radiation induced oxide-trapped charge can be enhanced by increasing temperature [56]–[60], [62], the current total ionizing dose test guidelines (TM 1019 and BS 22900) require devices to be kept at room temperature during irradiation and pre- and post-irradiation electrical characterization to minimize temperature-induced annealing effects. Because of this, the radiation response of devices are often not characterized over the full system temperature range. However, it has recently been shown that by not characterizing the radiation response of devices over the full system temperature range, the total-dose hardness of some devices can be overestimated [136].

This is illustrated in Figure 35, where large increases in static power supply current (I_{DD}) with temperature were observed for 1M (128k×8) CMOS SRAMs fabricated by Cypress Semiconductor. These SRAMs were fabricated using a 0.25-μm 5-V bulk silicon technology with a 6-transistor cell design. Figure 35 is a plot of I_{DD} versus temperature for the SRAMs irradiated with 95-MeV protons at TRIUMF [137] at a dose rate of ∼14 rad(SiO_2)/s. The devices were irradiated at 25°C with V_{DD} = 5 V and characterized at 25°C and 80°C. SRAMs were first irradiated to a given total dose and then characterized at room temperature and then at elevated temperature. After the elevated temperature characterizations, the SRAMs were cooled to room temperature and then irradiated with protons to a higher total dose level. As is evident from the figure, increasing the measurement temperature resulted in an increase in post-irradiation I_{DD}. For example, at a total dose of 72 krad(SiO_2) the leakage current measured at 25°C was 2.5 mA and at 80°C was 5.1 mA. In addition to an increase in leakage current, increasing the measurement temperature also caused the SRAMs to functionally fail at lower total dose levels. At the highest total dose level investigated, 161 krad(SiO_2), the SRAMs were still functional when characterized at 25°C. However, when the SRAMs were characterized at 80°C they failed functionally at total dose levels above 72 krad(SiO_2). These results

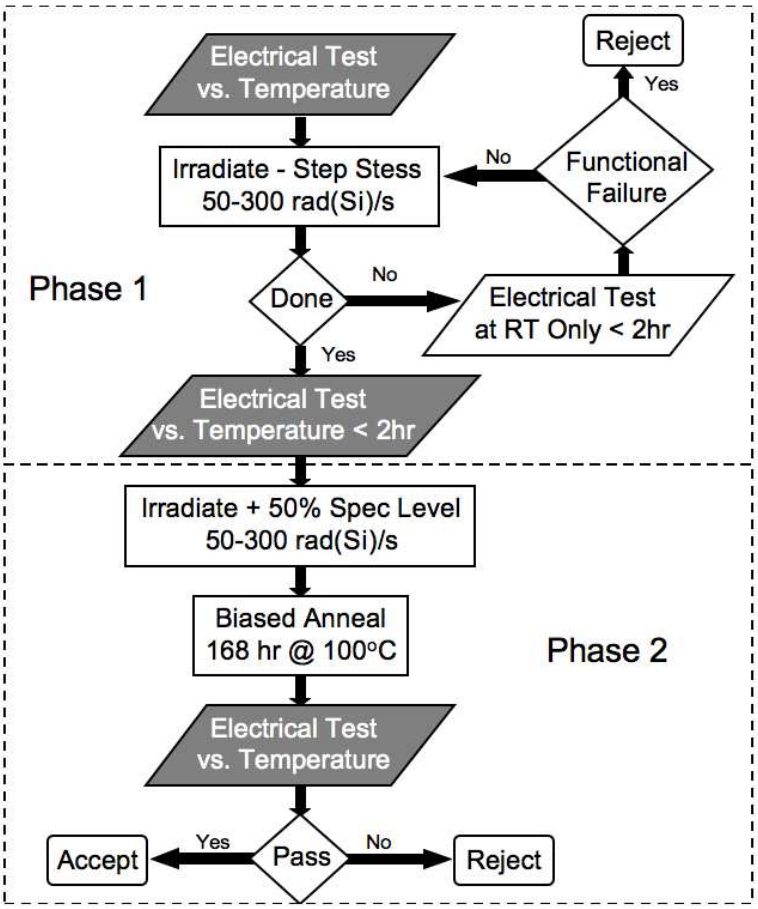

Fig. 36. Technique for integrating post irradiation temperature effects in a hardness assurance plan based on TM 1019. The shaded boxes highlight steps in the test procedure that could be modified to ensure device hardness over the system temperature range. (After [136].)

show the impact of characterization temperature on SRAM parametric and functional performance.

Ref. [136] also showed that transistors and a mixed-signal ASIC could exhibit significantly more post-irradiation parametric degradation when characterized at elevated temperatures. The results suggest that if elevated temperature operation is required for system application, it is imperative that devices be characterized at elevated temperatures, as well as at lower temperatures. The data of Figure 35 demonstrate a case where elevated temperature characterization caused increased parametric degradation and functional failure at lower total dose levels than room temperature characterization. It is possible that for other device types and/or technologies that enhanced parametric degradation and functional failure could be observed at cold temperatures. As a result, to ensure system functionality, it may be essential that devices be characterized over the the full system temperature range pre- and post-irradiation.

It is now illustrate how characterization tests over the temperature range of the system can be incorporated into TM 1019 (similar changes could be made to BS 22900). Figure 36 is a flow diagram based on TM 1019. Steps have been added to the flow diagram that could be used to ensure device hardness over the system temperature range. The devices should be characterized at room temperature and at the low and high temperature extremes of the system environment before irradiation. All devices should then be irradiated to the total dose specifications at a dose rate between 50 and 300 rad(Si)/s using a cobalt-60 gamma ray source, followed by electrical testing (Phase 1). If this is a step stress irradiation, the electrical testing should be done only at room temperature between each irradiation step. This is to ensure that minimal annealing of oxide-trapped charge occurs during the step stress.

Minimization of elevated temperature annealing can be very important to ensure that test Method 1019 remains conservative. It has been shown that the annealing rate (or neutralization) of oxide trapped charge can increase with temperature for some technologies [60], [62], [66], [138]. In addition, the buildup of interface traps also depends on temperature [63], [64]. Thus, because the purpose of Phase 1 of TM 1019 is to bound the degradation that is associated with the buildup of oxide-trapped charge, the most conservative approach to hardness assurance

testing is to not increase the temperature until after the completion of the irradiation sequence, unless it is known via characterization testing that the annealing of oxide-trapped charge and the buildup of interface-trap charge is insignificant for the parts being characterized. After the final total dose exposure of Phase 1, the devices should be characterized at room temperature and at the low and high temperature extremes. Note that the sequence for testing should be started at low or room temperature and end at high temperature. Again this will reduce the amount of oxide-trapped charge annealing that might occur. For high temperatures above 100°C, there is a possibility that some annealing of interface-trap charge might also occur [56]–[59]. However, the amount of annealing (if any) will be related to the amount of time that the devices are at temperatures above 100°C. Thus, this time should be minimized.

Phase 2 of Method 1019 then requires a 50% overtest, followed by a 168 hour, 100°C biased anneal. As such, any annealing of oxide-trapped charge that occurred during the last high temperature electrical test that was part of Phase 1 will have no negative impact on Phase 2 results. After the 1-week anneal, the devices should again be characterized at room temperature and at the low and high temperature extremes.

Using this revised hardness assurance test method we can better ensure that ICs will operate over the specified system temperature range in a given radiation environment. This is a more comprehensive test procedure compared to irradiating and testing devices only at room temperature. However, this test procedure does not take into account the fact that in an actual system application a device could also be irradiated at any temperature within the system environment specification. The effect of irradiating at a temperature other than room temperature and subsequently characterizing over the entire operating temperature range was not investigated in [136]. Thus, more work needs to done to fully investigate these effects to determine if the revised test method will bound the worst-case irradiation response of devices irradiated and operated over the entire specified temperature range, which should be the main objective of any test method. As is the case with the current test method, this revised test method may be overly conservative for predicting the radiation response of devices for some scenarios; however, it is impossible to develop a generic test method that is not overly conservative for some scenarios while still bounding the worst-case radiation response for devices that are specified to operate in a radiation environment over a wide range of temperatures (i.e., -55°C to 125°C) and dose rates.

The above discussion applies primarily to ICs with MOS elements. However, many bipolar devices are used in both space and weapons applications. Total dose radiation-induced degradation in these devices can also be attributed to the buildup of both oxide- and interface-trap charge in isolation oxides over the base-emitter junctions [82], [89] and emitter-base regions [83], [105]. Thus, it is not difficult to imagine that the radiation-induced degradation of bipolar devices can also be enhanced by testing at extreme temperatures. However, additional investigations will need to be conducted to determine if and to what extent the combined environment (radiation and temperature) will impact the radiation response of these device types. Until additional tests can be performed, it is recommended that bipolar devices also be characterized over the expected application temperature range after irradiation. Of course, as discussed above, this should be done at the end of the irradiation cycles to minimize annealing effects.

VI. Single-Event Effects Hardness Assurance Test Issues

A. Introduction

The harsh environments of space can induce single-event effects (SEE) in ICs. Both heavy ions and protons can cause SEE. Heavy ions induce SEE primarily by depositing charge by direct ionization along the path of the ions. Proton-induced SEE can be much more complex. The linear energy transfer (LET) of protons is not high enough to cause SEEs by direct ionization in most devices. Instead, protons induce SEE by generating secondary particles with much higher LETs, but with relatively low energies. Also, the secondary particles produced by proton-material interactions can be emitted in any direction (i.e., in general, they do not follow the path of the incident proton). These properties can lead to complex mechanisms for proton SEE and make hardness assurance testing difficult.

In memory circuits, information is stored at nodes in a circuit. If a high-energy heavy ion or proton reaction product strikes a circuit node, it can create sufficient charge in a transistor to change the state of the node and cause false information to be stored. This type of failure is a non-destructive or soft error and is known as a single-event upset (SEU). A soft error can be corrected by reprogramming the circuit into its correct logic state or by restarting an algorithm in a central processing unit. Another class of soft error is single-event functional interrupt (SEFI). A SEFI occurs when a device is switched into a nonfunctional mode, such as a test mode, a power-on reset

mode, or some other non-functional state. No permanent damage results, but the part may require a power reset or reprogramming before functionality returns. The soft error rate is normally specified in units of errors/bit-day. If the error rate is too large, it can result in performance degradation of a system and potentially mission failure.

A class of single-event effect that is not correctable by reprogramming is termed a hard error. Hard errors include single-event latchup (SEL), snapback (also called single transistor latch in silicon-on-insulator technology), burnout (SEB), and gate rupture (SEGR). Latchup is a high current condition that results from parasitic thyristor (SCR) action in 4-layer structures (e.g., CMOS ICs). Snapback is a high current, low resistance condition that occurs primarily in n-channel MOS transistors and is caused by impact ionization in the high electric field region near the drain junction. Both latchup and snapback can be triggered by large current transients created by the incident particle. Once a circuit is "latched up", large currents can flow, and remain unless the power supply to the circuit is interrupted. Unless the power supply current is limited, latchup and snapback can cause permanent damage to a circuit. Single-event burnout can cause permanent damage to bipolar power transistors and to power MOSFETs. A single-event gate rupture can occur as a single heavy ion or proton reaction product passes through a gate oxide, permanently damaging or destroying the gate oxide. SEGR occurs only at high oxide electric fields, such as those during a write or clear operation in a nonvolatile RAM or E^2PROM, or in a high-voltage power MOSFET. SEGR is caused by the combination of the applied electric field and the energy deposited by the ion.

There are a number of test guideline documents available in the U.S. on single event effects (SEE) testing. These include JEDEC Solid State Technology Association and ASTM (American Society for Testing and Materials) documents. JESD57 covers test procedures for the measurement of single-event effects in semiconductor devices from heavy-ion irradiation, JESD89 covers the measurement of alpha particle and terrestrial cosmic ray-induced soft errors in semiconductor devices, and ASTM F1192 covers standard guidelines for the measurement of single-event phenomena (SEP) induced by heavy-ion irradiation of semiconductor devices. These documents do a good job at defining the required procedures to follow for heavy ion SEE testing, although one must be vigilant as new effects are discovered that weren't anticipated in these documents. Currently there are no JEDEC, ASTM, or Mil-Std hardness assurance documents that specifically address proton SEE testing.

To characterize single-event effects, the number of events is measured as a function of heavy ion linear energy transfer (LET) or proton energy. For SEU, the number of events could be the number of bit upsets in a circuit. For SEL, the number of events could be the number of times a circuit was triggered into a latched high-current state. The device SEU-sensitive cross section is simply calculated as the number of events divided by the particle fluence. Heavy ion LET is varied by varying the ion and/or its energy. The effective LET can also be varied by changing the angle of incidence of the ion beam. As the angle of incidence is increased the path length of the ion through the sensitive volume (the volume of charge deposition that leads to single-event effects) will increase. The effective LET (LET_{eff}) at an angle of incidence Θ is given by

$$LET_{eff}(\Theta) = LET(0)/\cos(\Theta). \tag{3}$$

Heavy ion LET in the sensitive volume also depends on the type and thickness of overlayers in the device and the depth of the sensitive volume in the material. The effects of passing through various materials on LET can be calculated. Most automated heavy-ion SEE test facilities provide for this calculation as a part of their dosimetry. However, if the materials are not precisely known, it is best not to enter overlayer materials and thicknesses when performing the heavy-ion characterizations, but rather to record the incident LET at the device surface. Deconvolving the LET at the surface from the LET calculated assuming different overlayers and thicknesses can be extremely difficult.

It has recently been shown that very energetic heavy ions can generate secondary particles by heavy ion nuclear interactions with materials in an IC which can also lead to single-event effects (both SEU and SEL) [49], [139], [140]. The range of LETs of these secondary ions can vary widely. As a result, for instances where heavy-ion nuclear interactions are important, the basic concept of ion LET breaks down and one cannot generate a simple SEU (or SEL) cross section curve versus ion LET for regions where heavy-ion nuclear interactions dominate over direct ionization [49], [140].

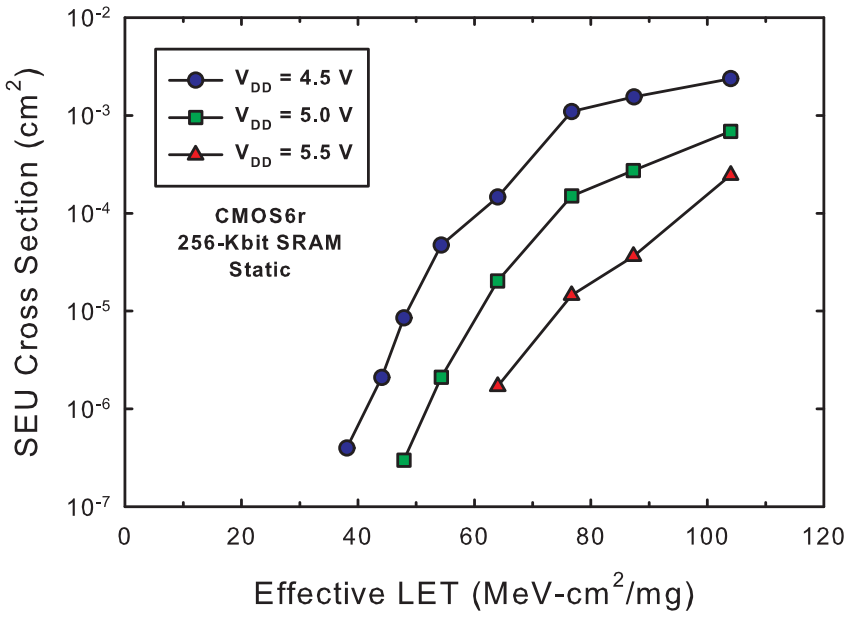

Fig. 37. Single-event upset cross section vs. heavy ion LET in Sandia 256-Kbit SRAMs with power supply bias voltage as a parameter.

B. Single-Event Upset (SEU)

The single-event upset sensitivity of devices depends on a number of operating conditions, including bias voltage, temperature, mode of operation (e.g., static vs. dynamic), angle of particle incidence, and others. For accurate and conservative estimates of error rates in a given application and environment, it is important to ensure testing is performed under the conditions that give the worst-case SEU response expected in the mission environment.

1) Bias Voltage: For the majority of devices, including standard bulk-silicon CMOS devices, the worst-case bias for SEU is the minimum power supply operating bias expected for the device in the system application, because this gives the minimum noise margin. Figure 37 shows an example of the impact of bias voltage on SEU cross section in Sandia bulk silicon 256-Kbit SRAMs manufactured using a 0.6-μm bulk silicon technology. As can be seen in this figure, bias voltage can have a substantial effect on SEU cross section, with minimum bias increasing SEU sensitivity. Note that if devices are to be qualified for general use or if the minimum operating bias for the system is unknown, then devices should be characterized at the minimum operating bias as defined by product specification. In general, system device requirements are the same or less stringent than product limits. It is possible that for some device types, minimum bias does not give worst-case conditions. For previously uncharacterized device types (e.g., bulk-silicon versus silicon-on-insulator devices), one should first determine the worst-case conditions for that device type. Once known, future testing of devices built in the same technology can be performed assuming the same worst-case conditions apply. For insulating technology devices (e.g. silicon-on-insulator), it should be determined that a high bias voltage condition does not represent a worst case condition due to parasitic bipolar gain effects.

2) Pattern/Vector Dependence: The irradiation pattern often used to test memory circuits is a logical checkerboard (CB), alternating by address and bit. Except for the all 0's or all 1's pattern, a logical checkerboard is often the easiest pattern to implement in a test algorithm. The use of physical data patterns, i.e., patterns that are related to the actual layout of the IC, rather than logical addressing is recommended where possible. These patterns can often provide further insight into the SEU sensitivity of the test IC, and allow the experimenter to check that errors are uniformly distributed. However, because layout information is generally proprietary to the IC manufacturer, it can be difficult to implement physical data patterns. In some cases, laser error mapping can be used to determine the logical to physical bit correspondence if such information cannot be obtained from the manufacturer.

Some devices, particularly dynamic RAMs and logic elements, have a preferred soft error failure mode, with either 0 to 1 or 1 to 0 transitions being more likely than the other. The selected test patterns should consider this possibility in their design. For SEU characterization when there is no prior knowledge of pattern dependence, a test

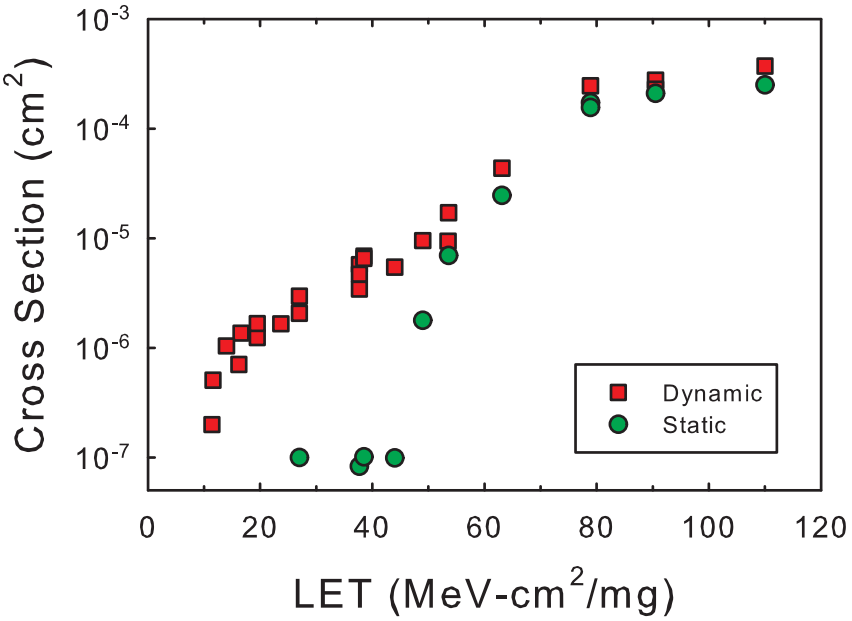

Fig. 38. Single-event upset cross section vs. heavy ion LET in 256-Kbit SRAMs tested statically and dynamically.

pattern that balances the number of 0s and 1s (such as a checkerboard pattern) is recommended. Since all 0's and all 1's patterns are easy to implement, it is also recommended to perform a quick check using all three patterns (CB, 0's, 1's) first to determine if there is any SEU pattern dependence before choosing a pattern for complete characterization.

For application-specific integrated circuits (ASICs) or microprocessors, the choice of test vector can be more problematic, since there is usually not a well-defined "generic" pattern that can be used. For these devices, it is highly desirable to use test vectors that closely approximate the system application that will be used on-orbit. Failing this, test vectors that provide the most complete coverage of possible failure modes are recommended to avoid missing a sensitivity that might not be detected with less complete test vectors. Selection of test vectors for ASICs therefore requires close coordination with the ASIC design team.

3) Static vs Dynamic Characterization: For memory technologies, static testing is often used because of the ease with which the test program can be written and the fact that timing issues from operating over long cables can be alleviated. In a static memory test, the memory is written to a given pattern, an irradiation sequence is performed, and after the irradiation is complete the memory is read and checked for errors. The problem with this method is that if there are upset modes that only exist during dynamic operation (for example, there are SEE-sensitive timing windows only open during dynamic operation), these upset modes will not be found. Also, if there is circuitry only active during dynamic operation, sensitivities in this circuitry will also not be found. Finally, static tests give no direct indication of multiple-bit upset sensitivity, since timing information is compressed into a single bit error map. Conversely, dynamic error maps can indicate (within the time resolution of consecutive error maps) whether multiple bits are failing within a single time window.

Figure 38 shows SEU cross section curves for a 256-Kbit SRAM taken using static and dynamic tests. Static testing was performed as described above (write once, irradiate, read once), while dynamic testing was performed by writing the memory, entering a read loop through the memory, irradiating the device while still reading continuously through the memory and counting errors. If errors are encountered during the irradiation, the failing bits are re-written on the fly until the irradiation is complete. In this example, the output buffers of the SRAM were sensitive to SEU, but were only exercised during the dynamic tests, so the sensitivity could not be detected during static tests.

For many classes of ICs only dynamic tests can be performed, because there is no static mode of operation possible. Of course, to fully characterize ICs in all the different possible test conditions is often not possible because of budgets and time constraints. For example, synchronous DRAMs may have many distinctly different

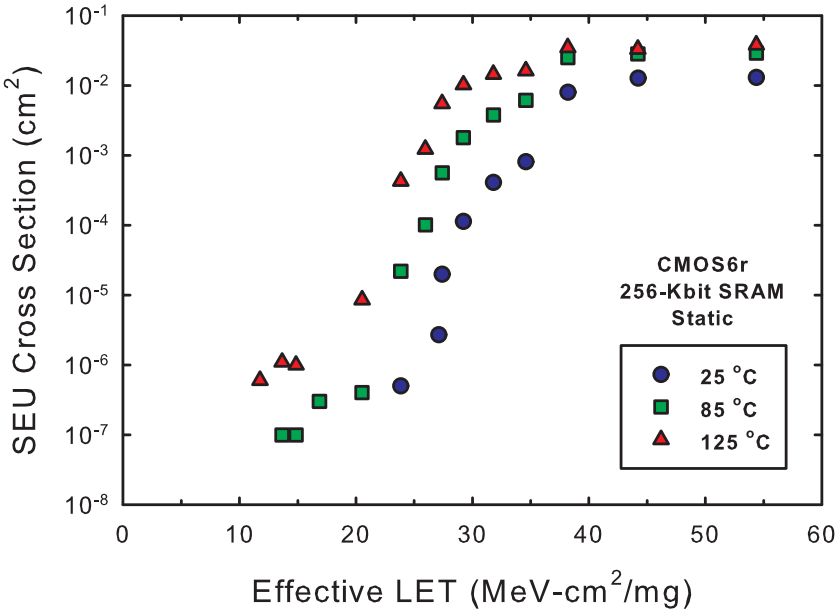

Fig. 39. Single-event upset cross section vs. heavy ion LET in Sandia 256-Kbit SRAMs with temperature as a parameter.

modes of operation. For this reason it is important to work with the end users to develop test conditions that closely match actual system use conditions. Unfortunately, since part selection and radiation qualification are often performed concurrently with system application development, using real flight application software is usually not an option.

4) Temperature: In general, SEU testing can be performed at room temperature. However, if passive elements have been designed into the ICs that are known to be temperature sensitive, any change in the operating temperature could impact the SEU hardness. For example, lightly-doped polysilicon feedback resistors are often used to improve SEU hardness of ICs. Lightly-doped polysilicon resistors have a negative temperature coefficient of resistivity, with lower resistance values at high temperatures than low temperatures. Thus, for polysilicon resistor-hardened technologies, maximum system temperature is worst case [141]. Figure 39 shows an example of the impact of operating temperature on SEU cross section in Sandia bulk silicon 256-Kbit SRAMs. These SRAMs use polysilicon feedback resistors and therefore their SEU performance degrades as temperature is increased. If one does not know if temperature impacts the SEU hardness of a given IC, it is prudent to perform some initial characterization as a function of temperature to determine the worst-case operating temperature for SEU.

Two basic techniques for performing SEU measurements at elevated temperatures are placing the device or subsystem under test within an enclosed temperature chamber, or applying heat locally to an individual IC(s) using resistive strip heaters. For example, an aluminum enclosure containing the device under test can be heated by blowing air into the enclosure with a variable-temperature hot air gun. This method works for proton testing, where the particles are able to penetrate through the enclosure material. Temperature gradients in such a setup can be fairly large, and methods to characterize and maximize temperature uniformity are important for repeatable results. Alternatively, resistive strip heaters can be mounted directly beneath or on top of an IC package, although ensuring good heat transfer to the device under test can be challenging depending on package/socket/board configuration. An advantage of resistive heating systems is that they are easier to control with temperature control units that automatically adjust heater power based on temperature sensor inputs.

In any event, accurate temperature measurements are key to repeatable SEU testing at elevated temperatures. Simply mounting a thermocouple to the test board can result in significant temperature error. By mounting a thermocouple directly to the device package, more accurate measurements can be obtained, but these still dont directly correspond to the actual die temperature inside the package. One method for achieving accurate and repeatable temperature measurements is to characterize input diode forward voltage for a given current as a function

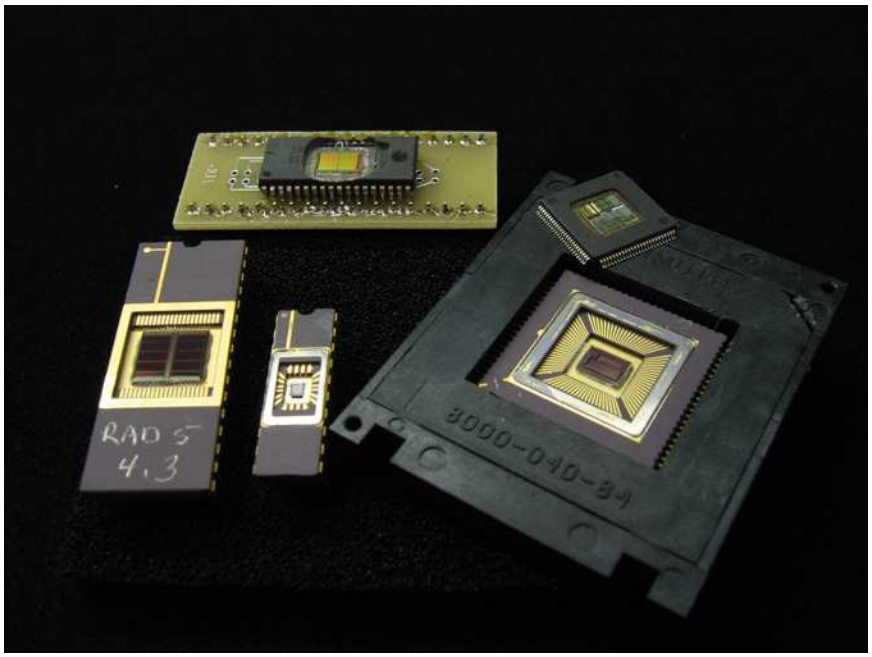

Fig. 40. Integrated circuits prepared for heavy-ion testing by removing package lids or etching away plastic mold compound.

of temperature. This can be done by placing the device in a well-characterized oven before the test and measuring the diode forward voltage as the oven temperature is varied. Since the diode voltage is strongly dependent on the die temperature, this method gives a sensitive measurement of the actual die temperature and can be performed prior to the test, with plenty of time allotted for the device to stabilize at the oven temperature.

5) Device Preparation: The ranges of heavy ions from laboratory radiation sources are normally small (tens to hundreds of microns) compared to package dimensions, therefore it is necessary to de-package ICs prior to testing. For devices packaged in ceramic packages, it may be possible to remove package lids, while devices in plastic packages require etching away the plastic mold compound encapsulating the active IC die. Figure 40 shows examples of integrated circuit packages prepared for heavy ion testing. In the foreground of the photograph are ceramic packages with the metal lids of the die removed to provide access, while in the background are two plastic-encapsulated devices that have had their mold compound removed by chemical etching. Once devices are delidded, special care must be taken to ensure that the devices are not damaged before testing. For proton testing, de-packaging ICs is not usually necessary since protons with energy greater than $\sim$30 MeV are capable of penetrating packaging materials. In fact, one of the advantages of proton testing is that quite often, subsystem-level testing can be performed without exposing the component die located inside the subsystem. However, low-energy ($\leq$30 MeV) proton testing requires that the die be exposed by de-packaging, similar to heavy ion testing.

6) Particle Energy: Single-event upset depends on the energy of both heavy ions and protons. For heavy ions, the energy must be high enough such that the ion can penetrate deep enough into the active region of the semiconductor with sufficient LET to capture all mechanisms that can lead to SEU. Failure to do so can lead to erroneous results. Note that if the mechanisms for SEU are not captured, even significant overtests will not ensure part functionality in space. The maximum energies of heavy ions achieved by most ground-based accelerators is generally in the range of 1-100 MeV/u. However, as mentioned earlier heavy ions in space typically have peak flux between 100 and 1000 MeV/u and are usually only weakly attenuated by spacecraft shielding. For some devices with moderate to high SEU thresholds, high energy ions can also cause nuclear interactions creating secondary particles that can trigger SEU for incident ions with LETs below the apparent LET threshold; whereas, lower energy ions may not trigger SEU. Because of these effects, for any given LET, the worst-case ion energy is the highest ion energy. All heavy-ion radiation sources will provide users with the range of ions in materials. The simplest method for determining the depth of active regions, overlayer thicknesses, etc. is to contact the manufacturer. However, because manufacturers are usually reluctant to give specifics of device fabrication, determination of depths of active regions, overlayer thicknesses can often only be obtained from destructive physical analysis of sample devices. The ranges

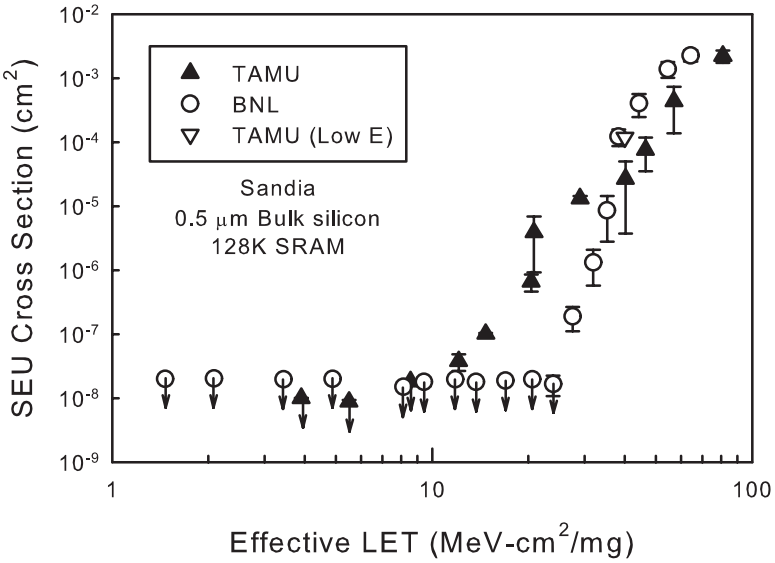

Fig. 41. Measured SEU cross section for 128-Kbit Sandia SRAMs taken with low-energy (BNL) and high-energy (TAMU) heavy ions. (After [145].)

of the ions used for heavy-ion characterization should always be much larger than the depths of the active regions. Failure to ensure this can lead to erroneous results. This should be done before selecting the radiation facility used for hardness assurance testing. The ranges of ions obtainable from some radiation facilities are not sufficient for ensuring that all failure mechanisms are captured. This is especially true for advanced IC technologies which can have very thick overlayers of oxides and metals. As a general rule, we recommend testing at the highest energy facility that is readily available.

Recently, an additional concern regarding high-energy heavy ions has been raised, namely, that of nuclear interactions between high-energy ions and the materials in integrated circuits [49], [142]–[145]. Typically, SEUs due to heavy ions are assumed to result from direct ionization caused by the release of electron-hole pairs along the path of an energetic charged particle incident on a device or IC. This is in contrast to proton and neutron SEU, where upsets are attributed to ionization by reaction products (e.g., spallation products and Si recoils) produced indirectly by nuclear interactions between an incident energetic particle and the materials in the IC. In [142], Koga theorized that for heavy ions with very low LET (< 1 MeV-cm^2/mg), upsets caused by nuclear interactions might be observable if the threshold LET for upsets caused by direct ionization was high (for example, as would be the case for SEU-hardened SRAMs). Several recent experiments [49], [140], [143] support this mechanism, with high-energy heavy-ion upsets observed for LETs below what appears to be the direct ionization SEU threshold LET as determined from low-energy experiments. While the SEU cross sections for this mechanism are generally low, it has been predicted that this mechanism could still be a significant contributor to on-orbit error rates [146].

Figure 41 shows the results of recent low- and high-energy SEU characterization of a bulk silicon 128-Kbit radiation-hardened SRAM [145]. Data were taken using low-energy ($\sim$1-10 MeV/amu) ions at Brookhaven National Laboratory (BNL) and high-energy (15-40 MeV/amu) ions at Texas A&M University (TAMU). Data points with a downward-pointing arrow indicate the upper bounds on the SEU cross section for LETs at which no upsets were actually observed. The SEU threshold LET of these SRAMs measured using standard low-energy ions is $\sim$28 MeV-cm^2/mg. In tests at BNL, no upsets were observed below an LET of $\sim$28 MeV-cm^2/mg, including repeated irradiations at an LET of 24 MeV-cm^2/mg with a cumulative fluence for all parts tested in excess of 2×10^8 ions/cm^2. These low-energy data indicate that if nuclear reaction-induced upsets in this technology exist, their cross section is less than 5×10^{-9} cm^2 at LETs less than 27.5 MeV-cm^2/mg. However, SEU data taken at TAMU indicate upsets still occur in these SRAMs with high-energy ions down to an LET of 12 MeV-cm^2/mg. In fact, at an LET of 12 MeV-cm^2/mg the high-energy SEU cross section is $\sim4\times10^{-8}$ cm^2, nearly a factor of ten higher than the *upper bound* for the low-energy SEU cross section at *twice* this LET! At an LET of 20 MeV-cm^2/mg, the high-energy SEU cross section is two orders of magnitude higher than the low-energy upper bound.

For LETs below the direct ionization upset threshold region, it therefore appears that at least in some cases

high-energy ions can lead to higher cross sections than low-energy ions [49], [143], [145]. It is generally accepted that this increase in SEU cross sections is attributable to nuclear reaction-induced upsets [140]. It appears that ion energy effects will be very difficult to observe in commercial (SEU-soft) devices because they are dominated by direct ionization [49], [142], [143]. Even in hardened devices, testing must be performed with very high fluences (we suggest $\geq 5{\times}10^7$ ions/cm^2) of heavy ions to observe this mechanism.

Unfortunately, differences in SEE response with ion energy due to secondary particles call many of our existing concepts for testing, understanding, and analyzing SEE into question. For example, the usefulness of the primary incident particle LET as a parameter against which SEU cross sections are plotted will be dramatically reduced. Because upsets may be caused by secondary particles with higher LET than the primary incident ion, plotting such secondary particle upsets against the incident ion LET is largely meaningless. In addition, the concept of effective LET breaks down as secondary particles don't follow an inverse cosine law based on the angle of incidence of the primary particle. Finally, many error rate prediction methods are implicitly based on charge deposition along path lengths of a primary ionizing particle passing through a sensitive volume. New methods based on an understanding of nuclear reaction cross sections will be required for cases where such reactions are important [144]. Testing at energies both above and below that required for nuclear reactions will likely be required to further refine these models [144].

For protons, the incident proton energy is the primary parameter that is varied when measuring the device upset cross section. Since for most ICs proton SEU is dominated by indirect ionization, the incident proton energy is very important since it determines what nuclear reactions may take place, their relative frequency, and the energy (and hence LET) of the secondary particles produced. High-energy protons can produce reaction products with higher LET than low-energy protons, and therefore it is important to perform proton testing at high enough energies to replicate the reactions expected to be observed in space environments. The maximum energy of protons encountered in the natural space environment is about 400 MeV. We recommend that whenever possible, proton SEU testing be performed using at least 180-200 MeV protons [147]. Testing should start at the highest proton energy to be evaluated and then at sequentially lower proton energies to obtain a complete upset cross section curve versus proton energy. This is because for the same fluence, the total dose deposited by high energy protons is less and high energy protons create less displacement damage than low energy protons. If the proton energy is lowered by degrading the energy of a high-energy beam line, proton energy dispersion effects (straggle) must also be taken into account. These effects can become significant as beam energy is degraded by factors of three to four or more and may result in erroneous results (i.e., the uncertainty in the proton energy is too large to accurately determine the SEU cross section versus proton energy).

7) Particle Fluence: The particle fluence used for SEU testing is generally driven by the sensitivity of the part being tested, with sensitive parts requiring low fluence for complete testing while SEU-resistant parts may require high fluences to achieve statistically meaningful results. If possible, the particle fluence should be adjusted to obtain a statistically significant number of upsets (e.g., 100 upsets for a 1M-bit SRAM) for any given irradiation condition. Often, a minimum number of upsets of 100 is used because this corresponds to a statistical uncertainly of about 20 percent with a 95% confidence level. The flux may also have to be adjusted to ensure that the tester can respond quickly enough to the observed upsets, particularly if the device is operating dynamically during irradiation. In addition, the aggregate total dose accumulated during SEU characterization may cause device functional failure and may affect the measured upset cross section. However, this is much less of a problem for heavy ions than for protons (discussed below). For most test conditions, a given total dose of heavy ions has considerably less effect on device radiation-induced degradation as the same total dose of protons. This is a result of the differences in charge yield between protons and heavy ions. If the SEU cross section of the device under test varies with total dose, multiple devices may be required to obtain a complete and accurate SEU cross section versus proton energy curve. SEFIs can cause significant dead times (times during which the device sensitivity cannot be measured but during which the particle beam is still incident) and particle fluence received during this dead time must be subtracted from the total fluence to the device when determining the cross section.

8) Angle of Incidence: The impact of angle of incidence is considerably different between heavy ions and protons. To vary heavy ion effective LET, the angle of incidence is often varied because this is easier and faster to do than to change the heavy ion energy or species. Care must be taken to ensure that the sides of device packages, package wells, etc. do not shadow the incident ion beam. This can be done visually if laser light is used to align the ion beam onto the device (e.g., as is done at Brookhaven's tandem van de Graaff). Heavy ion shadowing effects

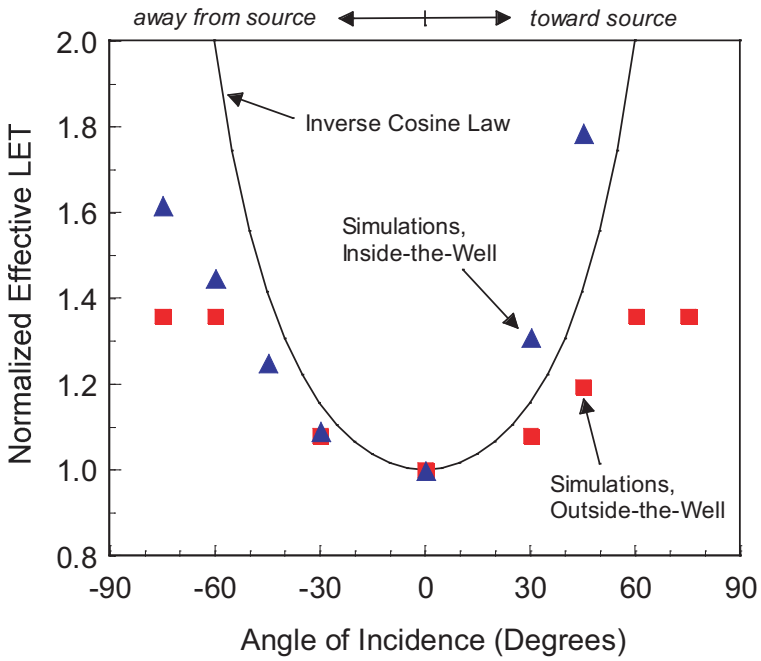

Fig. 42. Effective LET normalized to zero-angle LET for angled strikes to Sandia's CMOS6 technology. (After [148].)

can also be inferred by plotting error maps that show the physical location of errors observed in the particle beam. For ICs with a high degree of regularity in device layout (such as memories), the observed error map should show a uniform distribution of errors throughout the device. A lack of errors in one section of such a device is a strong indicator of device shadowing. The concept of effective LET can also break down due to geometric arguments at high angles of incidence [148]. This is illustrated in Figure 42, in which the effective LET (normalized to zero angle) as predicted by the effective LET inverse cosine law is plotted along with 3D simulation results for Sandia CMOS6 SRAMs. As can be seen in this figure, the inverse cosine law overestimates the effective LET predicted by by detailed 3D simulations. This is often seen in experimental SEU cross section data as high-angle data points that fall well below the expected curve, and discontinuities in the cross section curve as the ion beam is changed from large angles to normally-incident beams with similar LET. Because of this it is usually best to limit the concept of effective LET to a maximum angle of incidence of 45 degrees.

For most devices, proton angle of incidence does not have a significant effect on SEU cross section. Because secondary particles generated by proton/material interactions have relatively low energies, the range of the secondary particles can be much smaller than the depth of the SEU sensitive volume. Therefore, almost all of the charge deposited by secondary particles produced in the sensitive volume may be deposited within the sensitive volume, regardless of the angle of incidence, and the SEU cross section may be relatively independent of angle of incidence. However, this may not be true for all device structures (e.g., silicon-on insulator structures with very shallow sensitive volumes). Therefore, it is recommended that for protons at least a quick characterization as a function of angle (including grazing and back-side irradiation) be performed to ensure that the part is not angle sensitive. This can be done at a single proton energy (e.g., the maximum energy used for characterization, where proton energy losses are minimal).

9) Total Dose Effects: It has been shown that the SEU sensitivity of some devices can be degraded by exposing them to total ionizing dose [149]–[154]. This is illustrated in Figure 43 [149], which is a plot of the SEU cross section for 4M SRAMs irradiated with 35.4-MeV protons versus total dose. The cross section was determined from the incremental number of errors divided by the incremental fluence at each radiation level. These results show that the proton-induced SEU hardness of ICs can be significantly affected by total dose. For the total dose range examined, the upset cross section increases exponentially with total dose. The cross section increased from 7.9×10^{-9} cm^2 at a total dose of 1.1 krad(SiO_2) to 4.7×10^{-8} cm^2 at a total dose of 35.5 krad(SiO_2).

For older technologies with relatively thick oxides, the observed increased SEU sensitivity has been attributed to ionizing radiation-induced imbalances in the threshold voltages of the transistors within the memory cell [152]. The

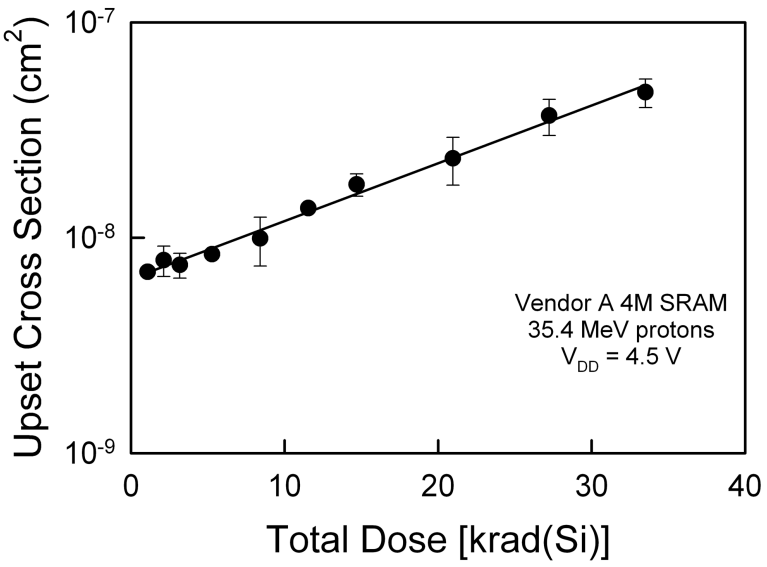

Fig. 43. Upset cross section versus total dose for 4M SRAMs. The devices were irradiated with 35.4-MeV protons with V_{DD} = 4.5 V. (After [149].)

magnitude of the radiation-induced threshold voltage shifts can be considerably different for ON and OFF biased transistors, leading to large imbalances in the threshold voltages. This mechanism is not expected to be a major problem for most present-day technologies that have very thin gate oxides in which there should be no significant amount of radiation-induced charge buildup. For these technologies (specifically for SRAMs), it has been suggested that the enhanced SEU sensitivity with total dose is consistent with radiation-induced currents originating in the memory cells affecting the output bias levels of bias level shift circuitry used to control the voltage levels to the memory cells and/or due to the lowering of the noise margin of individual memory cells caused by radiation-induced leakage currents [149]. In addition, all SRAMs that showed an enhanced SEU sensitivity, also showed a radiation-induced increase in the static power supply leakage current [154]. Thus, it may be possible to screen SRAMs for enhanced SEU sensitivity with total dose by monitoring changes in the static power supply leakage current with radiation. For other device types, the optimum parameter that needs to be monitored with irradiation may be different than the static power supply leakage current.

This correlation between total dose degradation and SEU sensitivity has important implications for space applications where the total dose is due to either electrons or protons. From a hardness assurance perspective, it is important that devices that exhibit this type of enhanced SEU sensitivity with ionizing dose be SEU characterized at the maximum total dose level expected during mission lifetime.

The first step in a hardness assurance test program should be to determine via characterization testing whether or not a device exhibits a correlation between total dose degradation and SEU sensitivity. To determine this, total-dose irradiations can be performed by irradiating devices using Co-60 gamma rays, x rays, electrons, or protons prior to proton or heavy-ion SEU testing. If protons are used, care should be taken to ensure that the proton energy is below the SEU proton threshold for the devices to prevent the devices from changing bias states. It has been shown that the SEU sensitivity will depend on the irradiation bias configuration [154]. For example, the worst-case response for an SRAM could be with the device irradiated and characterized with the same pattern written to the memory array or with the devices irradiated with one pattern and characterized with the complement pattern. This is illustrated in Figure 44 [154]. This figure is a plot of the SEU cross section versus total dose for commercial SRAMs. All total-dose irradiations were performed with a checkerboard pattern written to the memory array. The SEU cross section was measured with either a checkerboard or checkerboard complement pattern. The data show that the effect of total dose on SEU cross section depends strongly on the pattern written to the memory array during irradiation and SEU measurement. For these devices and test conditions, the memory pattern written to the memory array made more than two orders of magnitude difference in cross section at the highest total dose level. In addition, the time between total-dose irradiation and SEU characterization should be kept as short as possible to minimize possible room temperature annealing effects. For proton SEU characterizations, total-dose irradiating

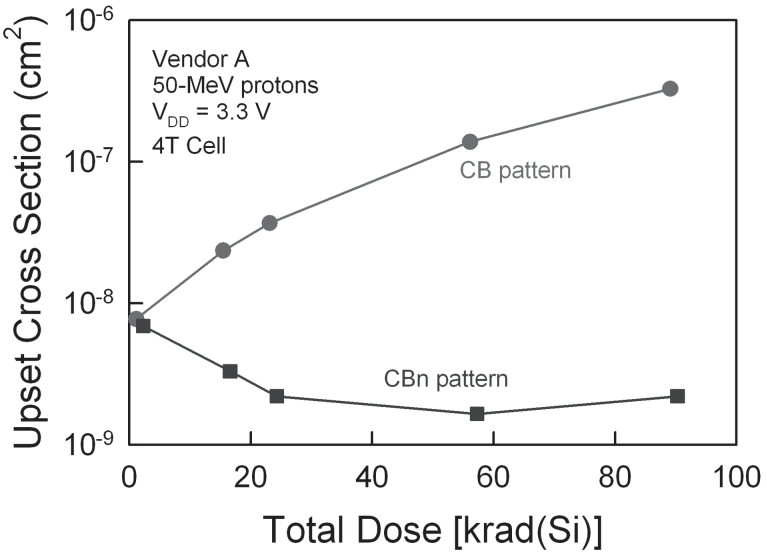

Fig. 44. Upset cross section versus total dose for commercial 4-Mbit SRAMs. The devices were irradiated with 50-MeV protons with V_{DD} = 3.3-V in a checkerboard pattern and characterized in either a checkerboard or checkerboard complement pattern. (After [154].)

devices with protons can easily meet this condition. For heavy-ion SEU characterizations, this condition may be difficult to meet for heavy-ion facilities without available total-dose facilities.

If hardness assurance qualification needs to be done on devices that show increased SEU sensitivity with ionizing dose, the irradiations prior to SEU characterization should be conducted using the irradiation conditions that bound the total dose degradation expected in the system environment. This can be done by following the basic principles of TM 1019 (see section II-A). As specified by the first phase of TM 1019, the devices could be irradiated using worst-case bias conditions to the maximum total dose at a moderate dose rate of 50 to 300 rad(SiO_2)/s. Of course this part of TM 1019 is a conservative test for parametric or functional failure due to radiation-induced oxide-trapped charge buildup, which can induce increases in static power supply leakage current. As such, this phase of the test will bound the radiation-induced increase in static power supply leakage current at moderate- to low-dose rates. However, as indicated above, this phase of TM 1019 is known to be overly conservative for estimating the response of the device and thus the method allows one to perform extended room temperature anneals to better estimate the parametric performance of devices at low dose rates [65]–[67]. The time for room temperature anneals is limited to the maximum time calculated by dividing the total ionizing dose specification for the devices by the maximum dose rate for the intended use. Following the room temperature anneals, the SEU response of the device can then be evaluated.

Extreme caution must be used if devices are subjected to the second phase of TM 1019 (rebound test) prior to SEU characterization. While there may be some device types that have a total dose sensitivity due to variations in interface-trap buildup affecting SEU hardness, to date, the total dose sensitivity for present-day SRAMs has been related to increases in static power supply leakage current. For MOS devices, increases in static power supply leakage current are due to radiation-induced increases in oxide-trapped charge. The part of TM 1019 which bounds the degradation due to the radiation-induced buildup of oxide-trapped charge is phase one. The elevated temperature anneals associated with phase two can significantly ”over anneal” the amount of oxide-trapped charge compared to what could be observed in the actual application and hence, greatly underestimate the increase in radiation-induced power supply leakage current even at low dose rates. Therefore, unless it is known that the total dose sensitivity is due to the radiation-induced buildup of interface traps, it is highly recommended that devices be subjected only to phase one of TM 1019 prior to SEU characterization.

A second option is to just irradiate the devices using the worst-case bias condition at low-dose rate before SEU characterization. While the exact rate to use is not known, a reasonable dose rate might be less than or equal to 10 mrad(SiO_2)/s. This is the dose rate required to test bipolar devices that might have ELDRS. While there are currently no data available on the impact of total dose on the SEU sensitivity of bipolar devices, it is known that the enhanced degradation (due to ELDRS) appears to saturate at dose rates below approximately 10 mrad(SiO_2)/s

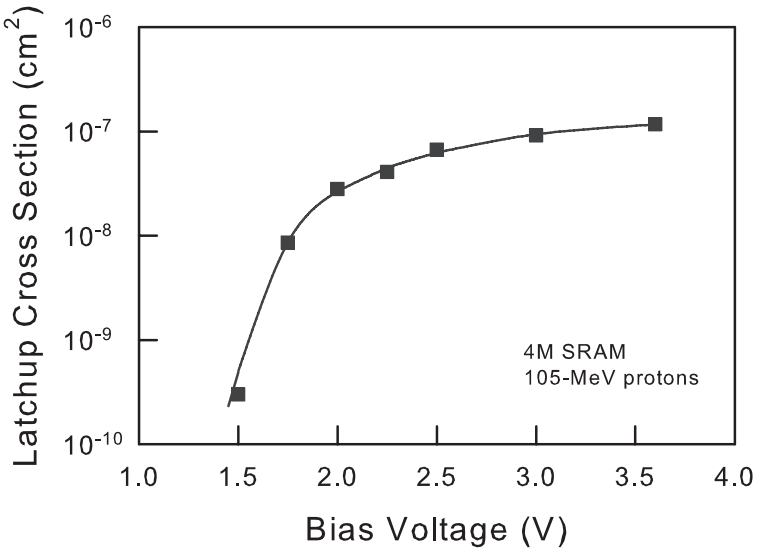

Fig. 45. SEL cross section versus bias voltage for SRAMs irradiated with 105-MeV protons.

[93]. For MOS devices, this dose rate also seems reasonable. It is still significantly higher than the rate expected for most space applications and if increases in static power supply currents are observed at 10 mrad(SiO_2), they will most likely exist at even lower dose rates.

C. Single-Event Latchup

One of the most problematic single-event effects is single-event latchup (SEL) [155]. When a latchup occurs, the latchup state can be cleared only by removing power from the device. SEL can also lead to destructive IC failure. As a result, many systems cannot tolerate even a single latchup or may require latchup circumvention (e.g., current limiting and/or fast reset capability) if there is a possibility of latchup. Thus, it is critical that hardness assurance tests for SEL be capable of accurately determining IC susceptibility to single-event latchup. While many of the same parameters are important for SEL as for SEU, some of these parameters have different (or even the opposite) effect for single-event latchup. SEL testing should be performed as described below to evaluate the probability of observing a latchup during system use.

1) Operating Bias: The effects of bias on proton and heavy-ion induced SEL have been explored in detail [155]–[157]. Based on these works, it is well known that the worst-case bias condition for both heavy-ion and proton-induced SEL is the maximum power supply voltage. This is illustrated in Figure 45, which is a plot of the SEL cross section versus bias voltage for 4M SRAMs with a nominal operating voltage of 3.3 V irradiated with 105-MeV protons. As the voltage is increased from 1.5 V to 3.6 V, there is approximately a three order of magnitude increase in the latchup cross section. SEL testing should therefore be performed at the maximum operating bias expected for the system. Note that if devices are to be qualified for general use or if the maximum operating bias for the system is unknown, then devices should be characterized at the maximum operating bias as defined by the product specification. In general, system device requirements are the same or less stringent than product limits.

2) Temperature: The effects of temperature on proton and heavy-ion induced SEL have also been reported [155]–[159]. The worst-case temperature for both heavy-ion and proton-induced SEL is maximum system temperature. Figure 46 is a plot of the latchup cross section for SRAMs measured at 25°C (room temperature) and at 85°C. For these SRAMs, the SEL maximum cross section is much higher at 85°C than at 25°C (three to four times higher at the highest proton energy). SEL testing should therefore always be performed at the maximum operating temperature expected for the system. Note that if devices are to be qualified for general use or if the maximum operating temperature for the system is unknown, then devices should be characterized at the maximum operating temperature as defined by product specification. System device requirements are usually the same or less stringent than product limits.

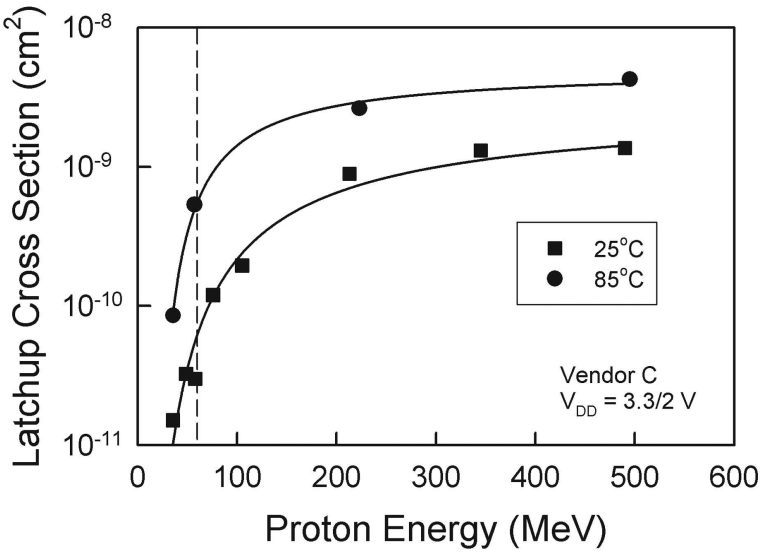

Fig. 46. SEL cross section versus proton energy for SRAMs characterized at temperatures of 25 and 85°C. (After [157].)

3) Device Preparation: Device preparation for SEL testing is essentially the same as for SEU testing, with delidded packages necessary for heavy ion tests and usually not necessary for proton tests. Because of the strong dependence of SEL on temperature, however, it is absolutely essential that testing be performed at the maximum system temperature. The device package and whether protons or heavy ions will be used play a role in choosing how to heat the parts during SEL testing. For dual-inline packages (DIPs) and many flat-pack packages, it may be possible to sandwich a resistive heater strip between the package and the test board, while pin and ball grid array packages may require heating from the top side of the package. For heavy ion testing, the necessity to leave the die exposed presents an additional constraint on the heating setup.

4) Particle Energy: Issues surrounding incident particle energy for SEL testing are similar to those for SEU testing. As for SEU, as a general rule we recommend testing at the highest energy facility that is readily available (proton or heavy ion). For heavy ions, the primary concern is ensuring the heavy ion energy is high enough such that the ion can penetrate deep enough into the active region of the semiconductor with sufficient LET to cause SEL. This is especially critical for SEL, since the sensitive volume for SEL is generally believed to be deeper than for SEU, and because charge conduction and collection from deep within the substrate plays a role in initiating latchup [155].

For protons, it has recently been shown that the probability of observing SEL during proton SEE testing can be a strong function of the proton energy used for testing [157]. This is clearly illustrated in Figure 47 [157]. Figure 47 is a plot of the SEL cross section as a function of proton energy for SRAMs manufactured by different commercial vendors measured at 85°C. As illustrated in the figure, the SEL threshold and cross section is a strong function of the proton energy and can vary significantly between devices, ranging from SRAMs with low SEL thresholds and high cross sections to SRAMs with high SEL thresholds and low cross sections. In fact for vendor D and E SRAMs, the minimum proton energy required to observe SEL was 225 MeV and 495 MeV, respectively. These proton energies are higher than the energies available at many proton test facilities (typically between 60 and 200 MeV) used in the past to evaluate the SEL response of ICs. However, trapped protons in Earth's radiation belts can have energies as high as 400 MeV [118] and galactic protons can have energies as high as 1 GeV. Thus, for systems where latchups cannot be tolerated, latchup testing should be performed using protons with energies at least equal to the maximum proton energy of the system environment. Although the proton fluence levels required to observe latchup in vendor D and E SRAMs would be much higher than obtainable in most systems, if many of these SRAMs were used in a system, in aggregate, the total cross section would be much higher and could result in realistic latchup probabilities for some space environments [160]. Conclusively excluding the possibility of latchup in such systems would require irradiating SRAMs to still higher fluence levels, probably necessitating the characterization of many SRAMs to avoid total dose damage of individual SRAMs.

These results strongly suggest that proton SEL hardness assurance testing should be performed at the maximum

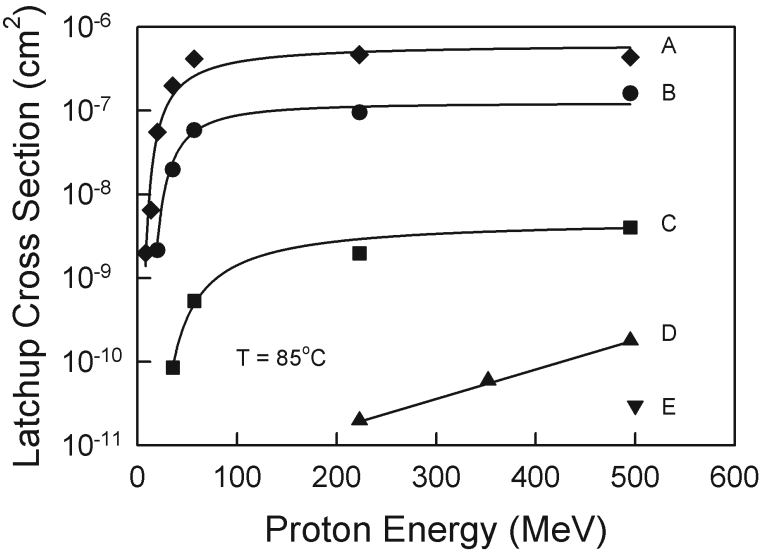

Fig. 47. Latchup cross section versus proton energy for five different SRAMs. SEL measurements were taken at a temperature of 85°C. (After [157].)

proton energy of the system environment. However, if no proton test facilities are available with proton energies at least equal to the maximum proton energy of the system environment, SEL testing may be performed using heavy ions with LETs greater than those expected from nuclear recoils generated by proton interactions. Remember that protons induce single-event effects through the generation of secondary particles with much higher LETs than those of the protons themselves. The maximum LET of secondary particles generated by proton-silicon interactions is approximately 11 MeV-cm^2/mg [161]. However, nuclear scattering cross section calculations for proton collisions with three high-Z materials (Cu, Ti, and W) common in many present-day high-density ICs show that secondary particles have a maximum LET of approximately 34 MeV-cm^2/mg for 500 MeV protons [157]. These data would suggest that if no SELs can be induced by heavy ions with LETs above $\sim$40 MeV-cm^2/mg, no SELs should be observed in a proton environment. Of course, as new high-Z materials are incorporated into technologies, nuclear scattering cross section calculations will need to be updated to ensure that no secondary particles with higher LETs can be generated. If no heavy ion SEL is observed at an LET of 40 MeV-cm^2/mg, no further testing would be warranted and the device can be considered to have passed SEL requirements. If heavy ion SEL is observed for LETs below 40 MeV-cm^2/mg, proton SEL testing will be required if it is still desired to use the part in a proton environment.

5) Angle of Incidence: Because proton-induced single-event latchup is typically caused by the generation of higher-LET secondary particles that can be emitted in all directions and have relatively low energies (penetration depths), the effect of angle of incidence can be considerably different for proton-induced SEL than for heavy-ion-induced SEL. For heavy ions, the angle of incidence can be varied to increase the effective LET, similar to heavy-ion-induced SEU. As before, care must be taken to ensure that the sides of device packages, package wells, etc. do not shadow the incident ion beam. In addition, the use of angled irradiations can exacerbate the issue of insufficient ion range to probe the SEL sensitive volume. The SEL cross section should follow roughly a $1/\cos(\Theta)$ dependence. If the SEL cross section follows this dependence at low angles of incidence, but significantly drops at higher angles of incidence, this is a good indication that shadowing effects are blocking the beam or the heavy ion range is insufficient.

For protons, the effect of angle of incidence on SEL cross section is illustrated in Figure 48, which is a plot of the SEL cross section versus proton energy for SRAMs irradiated at a temperature of 75°C at angles of incidence of 0 (normal angle) and 85 (grazing angle) degrees [162]. At each proton energy, the SEL cross section is larger for an angle of incidence of 85 degrees than for 0 degrees. This difference in SEL cross section between 0 and 85 degrees varies with proton energy. In fact, recent data show that at proton energies above 400 MeV, the angular dependence of proton SEL disappears. The difference in SEL cross section between low and high angles could easily affect the probability for detecting a latchup. Based on nuclear scattering calculations combined with 3-D

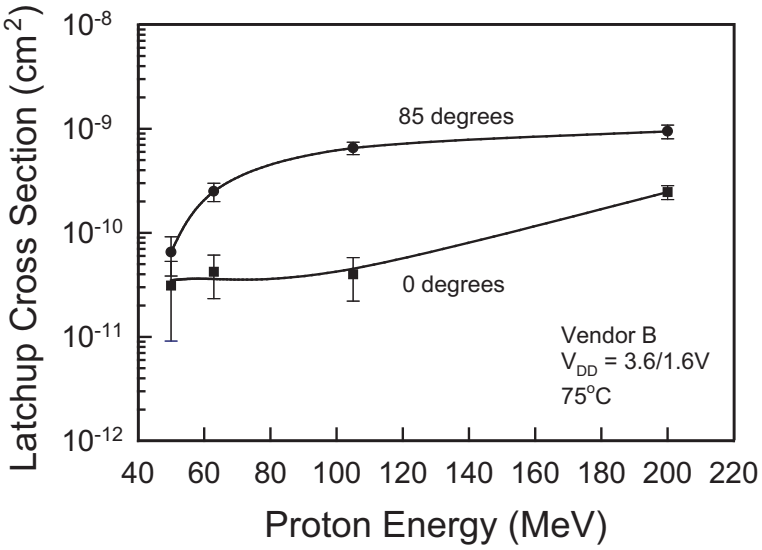

Fig. 48. Latchup cross section versus proton energy for SRAMs characterized at 75°C at angles of incidence of 0 and 85 degrees. (After [162].)

device simulations, it has been suggested that the mechanism for the effect of angle of incidence on SEL hardness is a consequence of the LET and range distributions of secondary ions produced by proton-material interactions, coupled with an increase in SEL sensitivity (decrease in LET threshold) as angle of incidence is increased [162].

At high proton energies ($\geq$400 MeV), testing needs to be performed at only one angle of incidence (typically with the proton beam at normal incidence to the device surface, 0 degrees). If testing is to be conducted at energies between 180 and 400 MeV, devices should be tested at a grazing angle of incidence between 80 and 90 degrees and at normal incidence. At proton energies below 400 MeV, the probability for SEL can greatly increase as the angle of incidence is changed from normal to grazing angle. However, because of energy losses as protons traverse the sides of packages, test fixtures, etc., testing should also be performed at normal incidence as an additional check.

6) Particle Fluence: The particle fluence used during SEL testing must be sufficient to establish with a high statistical confidence the probability that the device will or will not latch up in the intended system, especially since SEL has the potential to cause catastrophic failure of ICs. This fluence is dependent on system application. Although there is no strong evidence that either proton or heavy ion-induced total dose or displacement damage has a significant effect on SEL, total dose induced by high-fluence irradiations may increase the static operating current of the device to prohibitively large current values (or even cause functional failure). If continued device characterization causes prohibitively large increases in static current, multiple test devices may be required to reach the target fluence. If the SEL cross section is being characterized, the SEL cross section at the end of testing should be compared to the initial cross section to ensure that repeated testing has not changed the SEL cross section with accumulated total dose (fluence).

7) Latchup Characterization: Ideally, a latchup test should allow for both functional testing and current monitoring. Some parts are known to show only small increases in currents and without functional testing it may be difficult to detect such “microlatchups”. Functional tests can also be used to detect single-event snapback in SOI devices, where the increase in static power supply current can be small. By examining vector maps and by recycling the power supply, single-event latchups (and single-event snapback) can be distinguished from single-event upsets, single-event functional interrupts, etc. The large temperature dependence of latchup can also be used as a diagnostic aid to ensure that observed high-current states are truly due to latchup and not some other condition such as a bus contention issue. For cases where functional testing is not practical, devices can be characterized in their preferred power-up logic state, i.e., they do not have to be written with a specific pattern prior to exposure. For this case, the power supply current must be continuously monitored during irradiation. When the power supply current increases to above a preset limit a latchup is recorded. To measure a latchup cross section, multiple latchups must be recorded as a function of ion fluence. To measure multiple latchups, after a latchup is first recorded, the power supply voltage

must be quickly removed for a short period of time (e.g., 0.5 s) to clear the latchup state, the power supply voltage must be reapplied, and the latchup test can be continued. (Note that one must account for this dead time when determining the effective SEL cross section at a given ion LET. Also, to keep the dead time correction small the time between latchups should be much longer than the time period chosen for removing the bias.) The preset limit should be set to a current $\sim$10% above the static current for the device. Note that this current can change with temperature and total dose. As a result, it may have to be adjusted as testing continues or if the operating temperature is changed. In addition, to avoid catastrophic device failure caused by repeated latchup testing, the device current should be limited to a safe operating value. If functional testing is not possible at the test site, it is recommended that functional testing be performed post-test to ensure that the devices are still functional after irradiation and that the data are valid.

D. Single-Event Burnout and Single-Event Gate Rupture

Destructive SEE can occur in devices where high electric fields exist across oxides or doping junctions. For example, the high electric fields often present in power MOSFETs and nonvolatile memories during write operations and the device geometries of power MOSFETs make these devices more susceptible to SEB (power MOSFETs) and SEGR (power MOSFETs and nonvolatile memories) than standard CMOS devices. Typical operating voltages for CMOS devices, for example, are low enough to preclude the observance of SEB/SEGR in these devices [163], [164]. However, since there are exceptions and destructive failures have serious system-level implications, it is important to note that sudden permanent increases in current or functional failures may signal the occurrence of SEB/SEGR in any device type and should not be taken lightly. Although SEB and SEGR due to protons and neutrons have been reported, these effects are most commonly observed in heavy ion environments. In this document, we primarily concentrate on heavy-ion-induced SEB and SEGR in power devices.

Typical SEGR data taken for vertical power MOSFETs include the critical gate (and sometimes drain) field to dielectric breakdown as a function of LET [165]. Note that because SEGR is a destructive event, obtaining such data requires that many devices be destroyed during the experiment. Semi-empirical expressions that relate the voltage threshold for SEGR as a function of bias conditions, oxide thickness, and incident heavy ion LET have been developed for specific devices and fit measured SEGR data very well [165], [166]. Typical SEB data taken include the critical drain voltage to burnout as a function of LET. One fortunate difference between SEB and SEGR is that non-destructive test procedures exist for SEB. For example, a load resistor attached to the drain of a power MOSFET can provide current limiting and prevent destructive SEB [167]. Current pulses at the source can be counted as SEB events and the SEB cross-section can be non-destructively obtained as a function of either the drain voltage or the particle LET.

1) Operating Bias: SEGR occurs when the transient gate dielectric field following an ion strike exceeds a critical value and the gate dielectric becomes permanently damaged. Predictably, then, the static operating bias on the gate oxide is of prime importance to SEGR susceptibility. In vertical power MOSFETs, the drain bias also plays a role in SEGR, as the drain bias applied to the substrate can be transferred by the highly conductive heavy ion path to the vicinity of the gate dielectric, further increasing the transient electric field across the gate dielectric. The response due to the electric field directly across the gate is known as the “capacitor response,” while the response due to the drain bias on the substrate is known as the “substrate response” [168], [169]. Increasing the drain voltage decreases the gate voltage at which SEGR is observed for a given heavy ion. A simple relationship gives the capacitor response dependence of the SEGR critical field on the intrinsic oxide breakdown field (in the absence of a particle strike) and the heavy ion LET [170]:

$$E_{CR} = E_0/(1 + LET/B), \tag{4}$$

where E_0 is the intrinsic oxide breakdown field and B is a fitting parameter. A slightly more involved equation has been developed that also includes the dependence of the SEGR threshold gate voltage on the applied drain voltage [166]. Figure 49 shows a plot of the inverse of the critical oxide electric field necessary to produce SEGR as a function of heavy ion LET [163]. Fits to the data based on the equation above are shown as straight lines. Note that as the oxide thickness is decreased, the inverse critical field to SEGR for a given LET decreases, implying that thinner oxides have an increased SEGR tolerance.

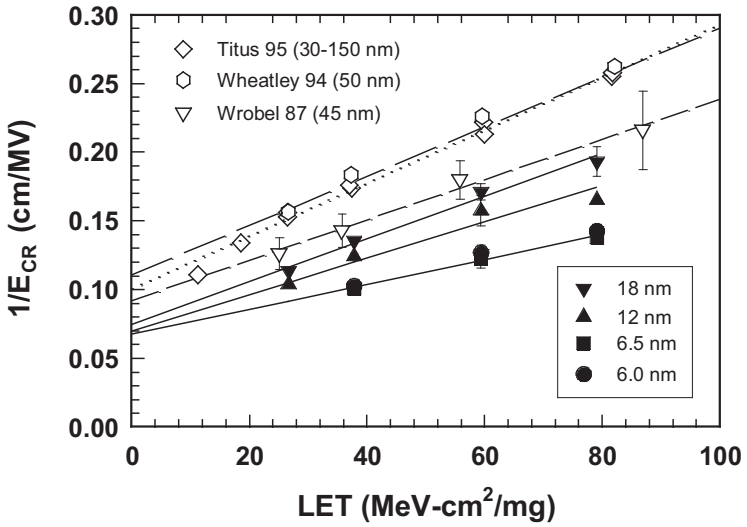

Fig. 49. Critical oxide electric field for SEGR as a function of heavy ion LET for several different oxides (After [163].)

SEB results in power MOSFETs when avalanching occurs in the high electric field region near the drain of the power MOSFET [171]. In an n-channel power MOSFET, electrons generated by an ion strike impact ionize in the high drain field, producing more electrons and holes. The holes must be removed by the p-body region, but as they leave they generate a voltage drop in the body region that forward biases the drain/body junction. This junction forms the emitter/base of the parasitic npn bipolar transistor inherent to n-channel power MOSFETs. As the drain/body junction becomes forward biased, the parasitic bipolar turns on, generating yet more electron current into the drain field region that can cause further impact ionization. As this regenerative process continues, the MOSFET can enter a thermal runaway condition, eventually leading to the burnout of the device. As with SEGR, this procedure is predictably worsened as bias (in this case, the drain voltage) is increased.

SEGR and SEB testing should be performed at the maximum operating bias expected for the system. For nonvolatile memories, this is the maximum bias during a write operation. For power MOSFETs, this is the highest gate-to-source voltage, V_{GS}, and highest drain-to-source voltage, V_{DS} for SEGR testing (source grounded) and it is the highest V_{DS} for SEB testing. For other device types it will be the maximum operating voltage. Note that if devices are to be qualified for general use or if the maximum operating bias for the system is unknown, then devices should be characterized at the maximum operating bias as defined by product specification. In general, system device requirements are the same or less stringent than product limits.

2) Temperature: SEGR is known to have little, if any temperature dependence [168], [172]. On the other hand, SEB sensitivity is known to decrease as temperature is raised, primarily because impact ionization is reduced with increasing temperature [173]. For these reasons, SEGR and SEB testing are usually performed at room temperature, although it could reasonably be argued that SEB testing should be performed at minimum expected system operating temperature.

3) Device Preparation: Because the ranges of heavy ions from laboratory radiation sources are normally small compared to package dimensions, it is necessary to de-package ICs prior to testing. This includes commercial devices in plastic packages. Because devices are delidded, special care shall be taken to ensure that the devices are not damaged before testing. As for SEU and SEL, it is generally not necessary to de-lid devices for proton-induced SEB or SEGR testing.

4) Ion Energy: The ion energy must be high enough such that the ion can penetrate deep enough into the active region of the semiconductor with sufficient LET to capture all mechanisms that can lead to SEGR or SEB. Failure to do so can lead to erroneous results. Note that if the mechanisms for SEGR or SEB are not captured, even significant overtests will not ensure part functionality in space. The impact of ion energy on SEGR in power MOSFETs has been fairly extensively studied [169], [174], [175]. In these works, it was shown that ion energy plays a strong role in the substrate response of power MOSFETs. The primary concern is that the ion energy must be high enough to ensure that the incident particles not only pass through the gate oxide of the device, but also

that they deposit charge through the full epitaxial region and into the heavily doped substrate. This is necessary because the charge track plays a crucial role in transferring the substrate (drain) bias up to the region near the gate oxide [174]. Insufficient ion range will underestimate the substrate response. However, total penetration of the epitaxial region by the test ion does not by itself ensure a worst-case condition, as the important parameter appears to be total charge deposition within the structure. Still, total penetration of the epitaxial region appears to be a necessary, if not totally sufficient, condition for accurate SEGR hardness assurance. Follow-on work in [169] seemed to suggest that the atomic number of the incident ion had a more direct influence than ion energy or LET on the capacitor response. Today it is generally accepted that maximizing charge deposition throughout the device structure will result in worst-case conditions [175], [176]. A detailed analysis of ion ranges and energies using the SRIM code has been performed to predict the worst-case ion energy for SEGR and incorporated into a suggested test protocol for vertical power MOSFET devices [177]. This protocol can be used to choose the worst-case test energy for a given incident particle for such devices. There is also some indication that SEGR may increase with ion energy for a given LET in capacitors [178]. As a general rule, maximizing LET while maximizing ion energy will be close to worst case.

5) Angle of Incidence: It has been known from early on that angle of incidence has an effect on SEB and SEGR sensitivity. However, unlike SEU, where sensitivity is increased with angle of incidence through the effective LET cosine law, both SEB and SEGR are worst-case for normally-incident particle strikes [163], [168], [172]. Therefore, SEGR and SEB characterization should be performed at normal incidence.

6) Ion Fluence: The ion fluence used during hardness assurance testing must be sufficient to establish with a high statistical confidence the probability that the device will or will not experience SEGR or SEB in the intended system(s). This fluence is dependent on system application. Although there is no strong evidence that either ion-induced total dose or displacement damage has a significant effect on SEGR or SEB [168], total dose induced by high-fluence ion irradiations may increase the static operating current of the device to prohibitively large current values (or even cause functional failure). If continued device characterization causes prohibitively large increases in static current, multiple test devices may be required to reach the target fluence. If the SEB cross section is being characterized, the SEB cross section should be compared to the initial cross section to ensure that repeated testing has not changed the SEB cross section with accumulated total dose (fluence).

7) SEGR Characterization: SEGR characterization is easily performed by monitoring the gate-to-source current, I_{GS}, for power MOSFETs and the static supply current, I_{DD} for nonvolatile memories. For other device types, monitoring the static supply current, I_{DD}, and checking device functionality may provide indications of SEGR sensitivity. SEGR is normally a destructive event and results in significant increases to the device current at very low voltages. As a result, if SEGR occurs, the device is often no longer usable. However, for some thin oxides, “soft breakdown” is observed, where the current increase is much smaller and the device or IC may actually still function properly but at an increased current level [179]. Because SEGR is usually destructive, it is extremely difficult to measure a cross section curve for SEGR. However, since a catastrophic failure due to SEGR could result in mission failure, usually SEGR cannot be tolerated and hence it is not important to obtain a complete cross section curve. Instead, mapping out the voltages and particle LETs at which SEGR becomes a possibility is usually sufficient.

8) SEB Characterization: SEB characterization is performed similarly to SEL testing by monitoring the I_{GS} and the drain-to-source current, I_{DS}, for power MOSFETs. These currents must be continuously monitored during irradiation. When either current increases to above a preset limit an SEB event is recorded. To measure an SEB cross section, multiple SEB events must be recorded as a function of ion fluence. To measure multiple SEB events, after a current spike is first recorded, all voltages must be quickly removed for a short period of time (e.g., 0.5 s) to clear the SEB state, the voltages must be reapplied, and the SEB test can be continued. (Note that one must account for this dead time when determining the effective SEB cross section at a given ion LET. Also, to keep the dead time correction small the time between SEB events should be much longer than the time period chosen for removing the bias.) The preset limit should be set to a current 10% above the static drain-to-source current for the device and to a current well above the static gate-to-source current (preset limits of microamps are generally sufficient for the gate-to-source current). To avoid catastrophic device failure caused by repeated SEB testing, the device current should be limited to a safe operating value. This is usually achieved by attaching a current-limiting load resistor to the drain of a power MOSFET [167]. The resistor value must be high enough to prevent either destructive burnout or non-destructive (but permanent) damage.

VII. Conclusion

Hopefully this document has given the reader the necessary background to understand the basics of radiation effects hardness assurance testing. Specifically, we've addressed: 1) What radiation environments a system might encounter in space. This is important for understanding what specific radiation tests might be needed to assure the performance of a system in a particular orbit. 2) What laboratory radiation sources are available. Combined with an understanding of radiation environments, this helps to understand what sources might be used for a radiation test campaign. 3) A brief description of how radiation interacts with electronic devices. This section helps set the stage for how devices respond to different types of radiation. 4) A few general test considerations of which the radiation hardness assurance engineer should be aware. 5) The nitty-gritty details of the impact of various test parameters on total dose and single-event effects device response. These details really get to the heart of what the reader may find in a test protocol, and why they're there. Our hope is that, armed with this information, the reader is able to understand how testing is done, how to interpret a test report and determine if it was a valid test or not, and what considerations to think about when specifying a test requirement for a system.

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